ALPHA DATA

ADMXRC3 API Hardware Addendum

Document Revision: 1.10
6th May 2016

	Head Office	US Office
Address:	4 West Silvermills Lane, Edinburgh, EH3 5BD, UK	3507 Ringsby Court Suite 105, Denver, CO 80216
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

Table Of Contents

List of Tables

1 Introduction

This document accompanies the ADMXRC3 API Specification 1.7.2, and provides information for application developers about how the hardware features of Gen 3 reconfigurable computing hardware are exposed via the ADMXRC3 API. In particular, it:

- Details the hardware features that are exposed via the ADMXRC3 API.
- Details hardware features that can be relied upon for all cards of the same model.
- Details hardware features that cannot be relied upon; for example, the end-of-life of a component may force new boards to be populated with a different but compatible device.

The information in this document applies to the following models:

- ADM-XRC-6TL
- ADM-XRC-6T1
- ADM-XRC-6TGE and ADM-XRC-6TGEL
- ADM-XRC-6T-ADV8 (board revision 2 and later)
- ADPE-XRC-6T and ADPE-XRC-6T-L
- ADPE-XRC-6T-ADV (board revision 2 and later)
- ADM-XRC-6T-DA1
- ADM-XRC-7K1
- ADM-XRC-7V1
- ADM-VPX3-7V2
- ADM-PCIE-7V3 (board revision 2 and later)
- ADM-XRC-KU1
- ADM-PCIE-KU3
- ADM-PCIE-8V3
- ADM-PCIE-8K5

1.1 Summary of hardware features for Virtex-6-based models

Table 1 below summarizes Virtex-6-based models currently supported by the ADMXRC3 API:

Feature	ADM-XRC-6TL	ADM-XRC-6T1	ADM-XRC-6TGE	ADM-XRC-6T-ADV8
Host interface	PCIe Gen 1 x4 [1]	PCIe Gen 2 x4 [1]	PCIe Gen 2 x4 [1]	PCIe Gen 2 x4/ x8 [1, 4]
PCI vendor ID	0x4144			
PCI device ID	0xADB3			
PCI subsystem vendor ID	0x4144			
PCI subsystem device ID	0x0201	0x0300	0x0301	0x0304
Model code	0x101	0x102	0x103	0x104
Number of programmable clock generators	1	0 or 1	3	0

Table 1 : Summary of hardware features for Virtex-6-based models **(continued on next page)**

Feature	ADM-XRC-6TL	ADM-XRC-6T1	ADM-XRC-6TGE	ADM-XRC-6T-ADV8
Number of DMA engines [2]	2	4	4	up to 4
Number of target FPGAs	1 x Virtex-6	1 x Virtex-6	1 x Virtex-6	1 x Virtex-6
Number of memory windows	4	4	4	4
Number of sensors [3]	10 or 13	10 or 13	13	16
Number of I/O module sites	1 x XRM	1 x XRM	1 x XRM	0
Number of memory banks	4	4	4	4
Number of Flash memory banks	1	1	1	1
Feature	ADPE-XRC-6T	ADPE-XRC-6T-L	ADPE-XRC-6T-ADV Controller	ADPE-XRC-6T-ADV Target
Host interface	PCIe Gen 2 x4 [1]	PCIe Gen 2 x1 [1]	PCIe Gen 2 x1 [1]	PCIe Gen 2 x4/ x8 [1, 4]
PCI vendor ID	0x4144			
PCI device ID	0xADB3			
PCI subsystem vendor ID	0x4144			
PCI subsystem device ID	0x0305	0x0303	0x0306	0x0307
Model code	0x105	0x106	0x107	0x108
Number of programmable clock generators	2	2	0	0
Number of DMA engines [2]	4	2	0	up to 4
Number of target FPGAs	1 x Virtex-6	1 x Virtex-6	2 x Virtex-6	1 x Virtex-6
Number of memory windows	4	4	4	4
Number of sensors [3]	21	21	18	0
Number of I/O module sites	1 x FMC	1 x FMC	0	0
Number of memory banks	2	2	8	4
Number of Flash memory banks	1	1	2	0
Feature	ADM-XRC-6T-DA1	ADM-XRC-6TGEL		
Host interface	PCIe Gen 2 x4 [1]	PCIe Gen 2 x1 [1]		
PCI vendor ID	0x4144			
PCI device ID	0xADB3			
PCI subsystem vendor ID	0x4144			
PCI subsystem device ID	0x0309	0x030A		
Model code	0x10A	0x10D		
Number of programmable clock generators	1	3		
Number of DMA engines [2]	4	4		

Table 1 : Summary of hardware features for Virtex-6-based models (continued on next page)

Feature	ADM-XRC-6T-DA1	ADM-XRC-6TGEL		
Number of target FPGAs	1 x Virtex-6	1 x Virtex-6		
Number of memory windows	4	4		
Number of sensors [3]	TBA	13		
Number of I/O module sites	1 x XRM	1 x XRM		
Number of memory banks	4	4		
Number of Flash memory banks	1	1		

Table 1 : Summary of hardware features for Virtex-6-based models

Notes:

[1] ADB3 PCI Express to OCP Bridge, implemented in a Xilinx FPGA.

[2] The number of DMA engines is permitted to increase with future firmware and/or driver updates; the values given here are minimum values.

[3] The number of sensors is permitted to increase with future firmware and/or driver updates; the values given here are minimum values. To maintain compatibility with existing software, the ordering of previously existing sensors is not permitted to change.

[4] The ADM-XRC-6T-ADV8 and ADPE-XRC-6T-ADV Target have a user-programmable Virtex-6 FPGA which serves both as the PCI Express host interface and the target FPGA for user applications. Hence, their PCI Express capabilities (Gen 1 vs. Gen 2, x4 vs. x8 etc.) are user-definable.

1.2 Summary of hardware features for 7 Series-based models

Table 2 below summarizes 7 Series-based models currently supported by the ADMXRC3 API:

Feature	ADM-XRC-7K1	ADM-XRC-7V1	ADM-VPX3-7V2	ADM-PCIE-7V3
Host interface	PCIe Gen 2 x4 [1]			PCIe Gen 3 x8 [4]
PCI vendor ID	0x4144			
PCI device ID	0xADB3			
PCI subsystem vendor ID	0x4144			
PCI subsystem device ID	0x0700, 0x0704	0x0701, 0x0703	0x0705	0x0706 [5]
Model code	0x109	0x10B	0x10C	0x10E
Number of programmable clock generators	2		2	2
Number of DMA engines [2]	4	4	4	up to 4
Number of target FPGAs	1 x Kintex-7	1 x Virtex-7	1 x Virtex-7	1 x Virtex-7
Number of memory windows	4	4	4	4
Number of sensors [3]	23	23	23	0 or 13
Number of I/O module sites	0	1 x XRM	1 x FMC	0
Number of memory banks	2	4	4	2
Number of Flash memory banks	1	1	1	1

Table 2 : Summary of hardware features for 7 Series-based models

Notes:

[1] ADB3 PCI Express to OCP Bridge, implemented in a Xilinx FPGA.

[2] The number of DMA engines is permitted to increase with future firmware and/or driver updates; the values given here are minimum values.

[3] The number of sensors is permitted to increase with future firmware and/or driver updates; the values given here are minimum values. To maintain compatibility with existing software, the ordering of previously existing sensors is not permitted to change.

[4] The ADM-PCIE-7V3 has a user-programmable Virtex-7 FPGA which serves both as the PCI Express host interface and the target FPGA for user applications. Using the Xilinx Integrated PCI Express Block for Virtex-7, it is capable of up to PCI Express Gen 3 x8.

[5] This is the PCI hardware ID if using Alpha Data's PCIe IP.

1.3 Summary of hardware features for Ultrascale-based models

Table 3 below summarizes Ultrascale-based models currently supported by the ADMXRC3 API:

Feature	ADM-XRC-KU1	ADM-PCIE-KU3	ADM-PCIE-8V3	ADM-PCIE-8K5
Host interface	PCIe Gen 2 x4 [1]	2 x PCIe Gen 3 x8 [5]		
PCI vendor ID	0x4144			
PCI device ID	0xADB3			
PCI subsystem vendor ID	0x4144			
PCI subsystem device ID	0x0808	0x0801 [4]	0x0805 [4]	0x0807 [4]
Model code	0x111	0x113	0x116	0x117
Number of programmable clock generators	3	6	3	4
Number of DMA engines [2]	2	up to 4	up to 4	up to 4
Number of target FPGAs	1 x Kintex Ultrascale	1 x Kintex Ultrascale	1 x Virtex Ultrascale	1 x Kintex Ultrascale
Number of memory windows	4	4	4	4
Number of sensors [3]	20	13	18	18
Number of I/O module sites	1 x XRM	0	2 x FireFly	2 x FireFly
Number of memory banks	4	2	2	2
Number of Flash memory banks	1	1	1	1

Table 3 : Summary of hardware features for Ultrascale-based models

Notes:

[1] ADB3 PCI Express to OCP Bridge, implemented in a Xilinx FPGA.

[2] The number of DMA engines is permitted to increase with future firmware and/or driver updates; the values given here are minimum values.

[3] The number of sensors is permitted to increase with future firmware and/or driver updates; the values given here are minimum values. To maintain compatibility with existing software, the ordering of previously existing sensors is not permitted to change.

[4] This is the PCI hardware ID if using Alpha Data's PCIe IP.

[5] The ADM-PCIE-KU3, ADM-PCIE-8V3 & ADM-PCIE-8K5 feature a PCIe edge connector with 16 PCIe Gen 3 lanes, which are bifurcated into two sets of 8 lanes. Up to two independent Gen 3 x8 PCIe cores can be instantiated in the FPGA.

2 Model codes

2.1 ADM-XRC-6TL

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x101 (ADMXRC3_MODEL_ADMXRC6TL).

2.2 ADM-XRC-6T1

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x102 (ADMXRC3_MODEL_ADMXRC6T1).

2.3 ADM-XRC-6TGE

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x103 (ADMXRC3_MODEL_ADMXRC6TGE).

2.4 ADM-XRC-6T-ADV8

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x104 (ADMXRC3_MODEL_ADMXRC6TADV8).

2.5 ADPE-XRC-6T

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x105 (ADMXRC3_MODEL_ADPEXRC6T).

2.6 ADPE-XRC-6T-L

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x106 (ADMXRC3_MODEL_ADPEXRC6TL).

2.7 ADPE-XRC-6T-ADV

The ADPE-XRC-6T-ADV is a composite device, consisting of a Controller device and 2 Target devices. Each device can be opened separately via the ADMXRC3 API.

2.7.1 ADPE-XRC-6T-ADV Controller

For the Controller device of an ADPE-XRC-6T-ADV, the **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x107 (ADMXRC3_MODEL_ADPEXRC6TADV_C).

2.7.2 ADPE-XRC-6T-ADV Target 0 / 1

For a Target device of an ADPE-XRC-6T-ADV, the **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x108 (ADMXRC3_MODEL_ADPEXRC6TADV_T).

2.8 ADM-XRC-7K1

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x109 (ADMXRC3_MODEL_ADMXRC7K1).

2.9 ADM-XRC-6T-DA1

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x10A (ADMXRC3_MODEL_ADMXRC6TDA1).

2.10 ADM-XRC-7V1

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x10B (ADMXRC3_MODEL_ADMXRC7V1).

2.11 ADM-VPX3-7V2

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x10C (ADMXRC3_MODEL_ADMVPX37V2).

2.12 ADM-XRC-6TGEL

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x10D (ADMXRC3_MODEL_ADMXRC6TGEL).

2.13 ADM-PCIE-7V3

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x10E (ADMXRC3_MODEL_ADMPCIE7V3).

2.14 ADM-XRC-KU1

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x111 (ADMXRC3_MODEL_ADMXRCKU1).

2.15 ADM-PCIE-KU3

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x113 (ADMXRC3_MODEL_ADMPCIEKU3).

2.16 ADM-PCIE-8V3

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x116 (ADMXRC3_MODEL_ADMPCIE8V3).

2.17 ADM-PCIE-8K5

The **Model** member of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex) has the value 0x117 (ADMXRC3_MODEL_ADMPCIE8K5).

3 Programmable clock generators

The information in this section applies to the following API elements:

- Member **NumClockGen** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- Information functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx.
- Clock management functions ADMXRC3_GetClockFrequency and ADMXRC3_SetClockFrequency.

Programmable clock generators, if present, have indices in the range 0 to *n*-1, where *n* is the value of the member **NumClockGen** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

3.1 ADM-XRC-6TL

The ADM-XRC-6TL has a single programmable clock with index 0, named LCLK (for historical reasons), as in Table 4 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVCMOS25	AY14	32 - 140	Clock synthesizer in PCIe to OCP Bridge

Table 4 : ADM-XRC-6TL clock generators

3.2 ADM-XRC-6T1

If the firmware revision lower than 1.6 (PCI revision 0x06), no clock generators are available.

If the firmware revision is 1.6 (PCI revision 0x06) or higher, and the driver version is 1.3.0 or higher, the ADMXRC3 API exposes a clock generator, implemented in the PCIe to OCP Bridge as in Table 5 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	AA31 (+) & AB31 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge

Table 5 : ADM-XRC-6T1 clock generators

3.3 ADM-XRC-6TGE & ADM-XRC-6TGEL

The ADM-XRC-6TGE and ADM-XRC-6TGEL expose 3 clock generators, as in Table 6 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	AA31 (+) & AB31 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge
1	LVDS25	M8 (+) & M7 (-)	5 - 312.5	SI5338 clock output 1
2	LVDS25	AF8 (+) & AF7 (-)	5 - 312.5	SI5338 clock output 2

Table 6 : ADM-XRC-6TGE & ADM-XRC-6TGEL clock generators

3.4 ADM-XRC-6T-DA1

The ADM-XRC-6T-DA1 exposes one clock generator, as in Table 7 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	AA31 (+) & AB31 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge

Table 7 : ADM-XRC-6T-DA1 clock generators

3.5 ADPE-XRC-6T & ADPE-XRC-6T-L

The ADPE-XRC-6T and ADPE-XRC-6T-L expose 2 clock generators, as in Table 8 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	K24 (+) & K23 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge
1	LVDS25	AB6 (+) & AB5 (-)	5 - 312.5	SI5338 clock output 1

Table 8 : ADPE-XRC-6T(-L) clock generators

3.6 ADM-XRC-7K1

The ADM-XRC-7K1 exposes 2 clock generators, as in Table 9 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	U27 (+) & U28 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge
1	LVDS25	J8 (+) & J7 (-)	5 - 312.5	SI5338 clock output 1

Table 9 : ADM-XRC-7K1 clock generators

3.7 ADM-XRC-7V1

The ADM-XRC-7V1 exposes 2 clock generators, as in Table 10 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	AJ32 (+) & AK32 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge
1	LVDS25	AK8 (+) & AK7 (-) AB8 (+) & AB7 (-) M8 (+) & M7 (-) C10 (+) & C9 (-)	5 - 312.5	SI5338 clock output 1

Table 10 : ADM-XRC-7V1 clock generators

3.8 ADM-VPX3-7V2

The ADM-VPX3-7V2 exposes 2 clock generators, as in Table 11 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	AJ32 (+) & AK32 (-)	5 - 700	Clock synthesizer in PCIe to OCP Bridge
1	LVDS25	A10 (+) & A9 (-) K8 (+) & K7 (-) Y8 (+) & Y7 (-) AH8 (+) & AH7 (-) AW10 (+) & AW9 (-)	5 - 312.5	SI5338 clock output 1

Table 11 : ADM-VPX3-7V2 clock generators

3.9 ADM-PCIE-7V3

ADB3 Driver 1.4.15 or earlier does not expose any clock generators for the ADM-PCIE-7V3.

ADB3 Driver 1.4.16 or later exposes 6 clock generators for the ADM-PCIE-7V3, as in Table 12 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25 DIFF_TERM	AE31 (+) & AF31 (-)	5 - 300	Reference clock Default 100 MHz
1	LVDS25 DIFF_TERM	AL29 (+) & AL30 (-)	5 - 300	Reference clock Default 250 MHz
2	N/A	T6 (+) & T5 (-)	5 - 300	SATA/SFP+ MGT reference clock Default 156.25 MHz
3	DIFF_SSTL15	AH15 (+) & AJ15 (-)	5 - 300, 342.857, 400, 480, 600	SODIMM 0 reference clock Default 400 MHz
4	DIFF_SSTL15	G30 (+) & G31 (-)	5 - 300, 342.857, 400, 480, 600	SODIMM 1 reference clock Default 400 MHz
5	N/A	V6 (+) & V5 (-)	5 - 300, 342.857, 400, 480, 600	SATA/SFP+ MGT reference clock Default 150 MHz

Table 12 : ADM-PCIE-7V3 clock generators

In the 5 - 300 MHz range, the actual frequency is the same as the requested frequency, due to the fact that the SI5338A permits highly accurate non-integer VCO division factors.

Above 300 MHz, clock generators 3, 4 and 5 can be programmed only for several discrete frequencies: 342.857, 400, 480 & 600 MHz. This is due to the fact that the SI5338A clock generator chip permits only integer VCO division factors when dividing by less than 8. As the VCO frequency used in the ADM-PCIE-7V3 is 2.4 GHz, the discrete frequencies are thus calculated as 2400/7, 2400/6, 2400/5 and 2400/4 MHz.

In the range where only discrete frequencies are allowed, ADMXRC3_SetClockFrequency will select the discrete frequency that is closest to that which is requested (i.e. minimising the absolute value of the error). For example, requesting 315 MHz results in an actual frequency of 300 MHz, and requesting 441 MHz results in an actual frequency of 480 MHz.

3.10 ADM-XRC-KU1

The ADM-XRC-KU1 exposes 3 clock generators, as in Table 13 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25 DIFF_TERM	AM19 (+) & AN19 (-)	5 - 700	Clock synthesizer in PCIe to OCP/AXI Bridge Default 200 MHz
1	LVDS25	Y32 (+) & Y33 (-) AA8 (+) & AA7 (-) AT10 (+) & AT9 (-)	5 - 312.5	PROGCLK0, PROGCLK1, PROGCLK2 (SI5338B clock output 1) Default 156.25 MHz
2	LVDS DIFF_TERM	AM21 (+) & AN21 (-)	5 - 312.5	FABRIC_CLK (SI5338 clock output 3) Default 300 MHz

Table 13 : ADM-XRC-KU1 clock generators

3.11 ADM-PCIE-KU3

The ADMXRC3 API exposes 6 clock generators for the ADM-PCIE-KU3, as in Table 14 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	N/A	K6 (+) & K5 (-)	5 - 300	Quad SFP+ 0 MGT ref. clock Default 156.25 MHz
1	N/A	L29 (+) & L30 (-)	5 - 300	Quad SFP+ 1 MGT ref. clock Default 156.25 MHz
2	LVDS25 DIFF_TERM	AA24 (+) & AA25 (-)	5 - 300	Reference clock Default 250 MHz
3	DIFF_HSTL_I	D23 (+) & C23 (-)	5 - 300, 342.857, 400, 480, 600	SODIMM 0 reference clock Default 400 MHz
4	DIFF_HSTL_I	AH18 (+) & AH17 (-)	5 - 300, 342.857, 400, 480, 600	SODIMM 1 reference clock Default 400 MHz
5	N/A	R29 (+) & R30 (-)	5 - 300, 342.857, 400, 480, 600	SATA MGT reference clock Default 150 MHz

Table 14 : ADM-PCIE-KU3 clock generators

In the 5 - 300 MHz range, the actual frequency is the same as the requested frequency, due to the fact that the SI5338A permits highly accurate non-integer VCO division factors.

Above 300 MHz, clock generators 3, 4 and 5 can be programmed only for several discrete frequencies: 342.857, 400, 480 & 600 MHz. This is due to the fact that the SI5338A clock generator chip permits only integer VCO division factors when dividing by less than 8. As the VCO frequency used in the ADM-PCIE-KU3 is 2.4 GHz, the discrete frequencies are thus calculated as 2400/7, 2400/6, 2400/5 and 2400/4 MHz.

In the range where only discrete frequencies are allowed, ADMXRC3_SetClockFrequency will select the discrete frequency that is closest to that which is requested (i.e. minimising the absolute value of the error). For example, requesting 315 MHz results in an actual frequency of 300 MHz, and requesting 441 MHz results in an actual frequency of 480 MHz.

3.12 ADM-PCIE-8V3

The ADMXRC3 API exposes 3 clock generators for the ADM-PCIE-8V3, as in Table 15 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	N/A	N33 (+) & N34 (-)	5 - 312.5	GTY_CLK_0B Quad SFP+ 0 MGT ref. clock Default 161.1328125 MHz
		U33 (+) & U34		GTY_CLK_0C Quad SFP+ 1 MGT ref. clock Default 161.1328125 MHz
1	N/A	AE33 (+) & AE34 (-)	5 - 312.5	GTY_CLK_1B FireFly 0 MGT ref. clock Default 161.1328125 MHz
		AJ33 (+) & AJ34		GTY_CLK_1C FireFly 1 MGT ref. clock Default 161.1328125 MHz
2	LVDS DIFF_TERM	G31 (+) & G32 (-)	5 - 312.5	MEM_CLK_0 DDR4 SDRAM bank 0 ref. clock Default 300 MHz

Table 15 : ADM-PCIE-8V3 clock generators (continued on next page)

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
2	DIFF_HSTL_II_18	AN25 (+) & AN26 (-)	5 - 312.5	MEM_CLK_1 DDR4 SDRAM bank 1 ref. clock Default 300 MHz

Table 15 : ADM-PCIE-8V3 clock generators

3.13 ADM-PCIE-8K5

The ADMXRC3 API exposes 4 clock generators for the ADM-PCIE-8K5, as in Table 16 below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	N/A	AE8 (+) & AE7 (-)	5 - 312.5	GTH_CLK_0 SFP+ 0 MGT ref. clock Default 156.25 MHz
1	N/A	AA8 (+) & AA7 (-)		GTH_CLK_1 SFP+ 1 MGT ref. clock Default 156.25 MHz
2	DIFF_SSTL12	G16 (+) & G15 (-)	5 - 312.5	MEM_CLK_0 DDR4 SDRAM bank 0 ref. clock Default 300 MHz
		AM22 (+) & AN22 (-)		MEM_CLK_1 DDR4 SDRAM bank 1 ref. clock Default 300 MHz
3	N/A	F10 (+) & F9 (-)	5 - 312.5	GTH_CLK_2 FireFly 1 MGT ref. clock Default 156.25 MHz

Table 16 : ADM-PCIE-8K5 clock generators

4 DMA engines

The information in this section applies to the following API elements:

- Member **NumDmaChannel** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- Information functions ADMXRC3_GetCardInfo and ADMXRC3_GetCardInfoEx.
- DMA functions ADMXRC3_ReadDMA, ADMXRC3_ReadDMAEx, ADMXRC3_ReadDMALocked, ADMXRC3_ReadDMALockedEx, ADMXRC3_WriteDMA, ADMXRC3_WriteDMAEx, ADMXRC3_WriteDMALocked and ADMXRC3_WriteDMALockedEx.
- Non-blocking DMA functions ADMXRC3_StartReadDMA, ADMXRC3_StartReadDMAEx, ADMXRC3_StartReadDMALocked, ADMXRC3_StartReadDMALockedEx, ADMXRC3_StartWriteDMA, ADMXRC3_StartWriteDMAEx, ADMXRC3_StartWriteDMALocked and ADMXRC3_StartWriteDMALockedEx and ADMXRC3_FinishDMA.

4.1 ADM-XRC-6TL

The ADM-XRC-6TL has 2 DMA engines, which are fully independent of one another.

In firmware **before** version 1.4 (PCI revision 0x04), the low 32 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine an addressing capacity of 4 GiB.

In firmware version 1.4 (PCI revision 0x04) and later, (at a minimum) the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of at least 512 GiB.

4.2 ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL, ADM-XRC-6T-DA1, ADM-XRC-7K1, ADM-XRC-7V1 & ADM-VPX3-7V2

The ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL, ADM-XRC-6T-DA1, ADM-XRC-7K1, ADM-XRC-7V1 and ADM-VPX3-7V2 each have 4 DMA engines, which are fully independent of one another. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

4.3 ADM-XRC-6T-ADV8

The ADM-XRC-6T-ADV8 has up to 4 DMA engines, which are fully independent of one another. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

Since the ADM-XRC-6T-ADV8 has a single Virtex-6 FPGA that serves both as the host interface and the target FPGA for user designs, each DMA engine consumes logic resources that might otherwise be used by the user application FPGA design. Alpha Data supplies default PCI Express IP to be embedded within a user FPGA design for the ADM-XRC-6T-ADV8 that in effect has 1.5 DMA engines:

- DMA engine 0 functions normally, and transfers data in either direction (FPGA to host and host to FPGA).
- DMA engine 1 transfers data only in the FPGA to host direction, saving some logic resources in the FPGA.

Alpha Data can supply PCI Express IP with a different DMA engine configuration on request.

4.4 ADPE-XRC-6T & ADPE-XRC-6T-L

The ADPE-XRC-6T has 4 DMA engines and the ADPE-XRC-6T-L has 2 DMA engines. Each DMA engine is fully independent of the others. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

4.5 ADPE-XRC-6T-ADV Target

The ADPE-XRC-6T-ADV Target device has up to 4 DMA engines, which are fully independent of one another. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

Alpha Data supplies default PCI Express IP to be embedded within a user FPGA design that has four DMA engines, and PCI Express IP with a different DMA engine configuration can be supplied on request.

4.6 ADM-PCIE-7V3

The **PCI Express to AXI4/OCP IP for the ADM-PCIE-7V3 & ADM-PCIE-KU3**, supplied by Alpha Data, can have up to four DMA engines. Each DMA engine is fully independent of the others. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

ADM-XRC Gen 3 SDK 1.7.0 and later includes a time-limited, evaluation version of the **PCI Express to AXI4/OCP IP for the ADM-PCIE-7V3**, which can be embedded within a user FPGA design. This has four DMA

engines. The time limit applies to the DMA engines; one hour after configuration (generally occurring at power-on) the DMA engines are disabled.

Customers who purchase the Reference Designs for the ADM-PCIE-7V3, available separately from the ADM-XRC Gen 3 SDK, gain access to unrestricted versions of the ADM-PCIE-7V3 PCI Express to AXI4/OCP IP. Please contact sales@alpha-data.com for further details.

4.7 ADM-XRC-KU1

The ADM-XRC-KU1 has 2 DMA engines, which are fully independent of one another. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

4.8 ADM-PCIE-KU3

The **PCI Express to AXI4/OCP IP for the ADM-PCIE-KU3**, supplied by Alpha Data, can have up to four DMA engines. Each DMA engine is fully independent of the others. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

Customers who purchase the Reference Designs for the ADM-PCIE-KU3 gain access to unrestricted versions of the ADM-PCIE-KU3 PCI Express to AXI4/OCP IP. Please contact sales@alpha-data.com for further details.

4.9 ADM-PCIE-8V3

The **PCI Express to AXI4/OCP IP for the ADM-PCIE-8V3**, supplied by Alpha Data, can have up to four DMA engines. Each DMA engine is fully independent of the others. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

Customers who purchase the Reference Designs for the ADM-PCIE-8V3 gain access to unrestricted versions of the ADM-PCIE-8V3 PCI Express to AXI4/OCP IP. Please contact sales@alpha-data.com for further details.

4.10 ADM-PCIE-8K5

The **PCI Express to AXI4/OCP IP for the ADM-PCIE-8K5**, supplied by Alpha Data, can have up to four DMA engines. Each DMA engine is fully independent of the others. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

Customers who purchase the Reference Designs for the ADM-PCIE-8K5 gain access to unrestricted versions of the ADM-PCIE-8K5 PCI Express to AXI4/OCP IP. Please contact sales@alpha-data.com for further details.

5 Target FPGAs

The information in this section applies to the following API elements:

- Member **NumTargetFpga** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- The structures ADMXRC3_FPGA_INFOA and ADMXRC3_FPGA_INFOW.
- Informational functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx, ADMXRC3_GetFpgaInfoA and ADMXRC3_GetFpgaInfoW.
- Target FPGA management functions ADMXRC3_ConfigureFromBuffer, ADMXRC3_ConfigureFromFileA, ADMXRC3_ConfigureFromFileW and ADMXRC3_Unconfigure.

Target FPGAs have indices in the range 0 to *n*-1, where *n* is the value of the member **NumTargetFpga** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

5.1 ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL & ADM-XRC-6T-DA1

The ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL and ADM-XRC-6T-DA1 all have a single target FPGA with index 0. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 17 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "6vlx240tff1759".
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1759	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 173 => ADMXRC3_FPGA_6VLX550T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1759"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 17 : Target FPGA 0 information for ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL & ADM-XRC-6T-DA1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.2 ADM-XRC-6T-ADV8

The ADM-XRC-6T-ADV8 has a single user-programmable FPGA with index 0, which serves both as the PCI Express host interface and the target FPGA. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW

respectively is detailed in Table 18 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "6vsx475tff1759".
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1759	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 173 => ADMXRC3_FPGA_6VLX550T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1759"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 18 : Target FPGA 0 information for ADM-XRC-6T-ADV8

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.3 ADPE-XRC-6T & ADPE-XRC-6T-L

The ADPE-XRC-6T and ADPE-XRC-6T-L each have a single target FPGA with index 0. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 19 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "6vlx365tff1156".
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1156	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 168 => ADMXRC3_FPGA_6VLX130T 169 => ADMXRC3_FPGA_6VLX195T 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1156"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 19 : Target FPGA 0 information for ADPE-XRC-6T(-L)

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.4 ADPE-XRC-6T-ADV

Logically, the ADPE-XRC-6T-ADV resembles a pair of ADM-XRC-6T-ADV8s "Target" devices with an extra Controller device whose function is monitoring and configuring the target devices. The two Target devices are not capable of monitoring or configuring themselves.

Information about the FPGA in a particular Target device can be obtained in one of two ways:

- By opening the Controller device via the ADMXRC3 API and then calling ADMXRC3_GetFpgaInfo or , specifying the index of the Target device of interest (0 or 1). This returns an ADMXRC3_FPGA_INFO structure whose content resembles that which would be returned had it been called on an ADM-XRC-6T1, ADM-XRC-6TGE etc. This case is covered in more detail in Section 5.4.1
- By opening the Target device of interest via the ADMXRC3 API and then calling ADMXRC3_GetFpgaInfo, specifying 0. This returns an ADMXRC3_FPGA_INFO structure whose content resembles that which would be returned had it been called on an ADM-XRC-6T-ADV8. This case is covered in more detail in Section 5.4.2

The difference between calling ADMXRC3_GetFpgaInfo on the Controller device versus on a Target device is

the difference in point of view. From the Controller's point of view, each of the two Target device FPGAs are considered to be reconfigurable. In contrast, from a Target device's point of view, it cannot reconfigure itself; nor does it have visibility of the other Target device.

In practical terms, the difference between calling ADMXRC3_GetFpgaInfo on the Controller device and calling ADMXRC3_GetFpgaInfo on a Target device is the presence or absence of the flag ADMXRC3_FPGA_NOTCONFIGURABLE in the returned ADMXRC3_FPGA_INFO structure.

5.4.1 ADPE-XRC-6T-ADV Controller

When calling ADMXRC3_GetFpgaInfo on the Controller device, the index of the Target FPGA of interest is passed in the **index** parameter of ADMXRC3_GetFpgaInfo, which can be 0 or 1. The returned ADMXRC3_FPGA_INFO structure contains the following information:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "6vsx315tff1759".
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1759	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 173 => ADMXRC3_FPGA_6VLX550T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1759"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 20 : FPGA 0 / 1 information for ADPE-XRC-6T-ADV Controller

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.4.2 ADPE-XRC-6T-ADV Target 0 / 1

When calling ADMXRC3_GetFpgaInfo on a Target device, the **index** parameter of ADMXRC3_GetFpgaInfo must be 0, because a Target device can only obtain information about its own FPGA. The returned

ADMXRC3_FPGA_INFO structure contains the following information:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "6vsx315tff1759".
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1759	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 173 => ADMXRC3_FPGA_6VLX550T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1759"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 21 : FPGA 0 information for ADPE-XRC-6T-ADV Target

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.5 ADM-XRC-7K1

The ADM-XRC-7K1 has a single target FPGA with index 0. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 22 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "7k410tffg900".
FamilyCode	7 => ADMXRC3_FAMILY_7SERIES	
SubfamilyCode	113 => ADMXRC3_SUBFAMILY_7KT	
PackageCode [1]	0x46460384 => FFG900	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 234 => ADMXRC3_FPGA_7K325T 236 => ADMXRC3_FPGA_7K410T	
Package [1]	"FFG900"	String indicating package type.
Flags	ADMXRC3_FPGA_SPEEDVALID	Indicates that SpeedGrade is valid; see ADMXRC3 API Specification for details of flags.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.
Stepping	""	String is empty because stepping is not defined for 7 Series FPGAs.
Present	TRUE	Should always be TRUE for normal cards.

Table 22 : Target FPGA 0 information for ADM-XRC-7K1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.6 ADM-XRC-7V1 & ADM-VPX3-7V2

The ADM-XRC-7V1 and ADM-VPX3-7V2 have a single target FPGA with index 0. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 23 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "7vx690tffg1761".
FamilyCode	7 => ADMXRC3_FAMILY_7SERIES	
SubfamilyCode	Varies according to device fitted: 114 => ADMXRC3_SUBFAMILY_7VT 115 => ADMXRC3_SUBFAMILY_7VXT	
PackageCode [1]	0x464606E1 => FFG1761	Numerical code indicating package type.

Table 23 : Target FPGA 0 information for ADM-XRC-7V1 & ADM-VPX3-7V2 (continued on next page)

Member	Possible values	Comment
Device [1]	Varies according to device fitted: 248 => ADMXRC3_FPGA_7V585T 249 => ADMXRC3_FPGA_7V1500T 250 => ADMXRC3_FPGA_7V2000T 256 => ADMXRC3_FPGA_7VX330T 258 => ADMXRC3_FPGA_7VX485T 260 => ADMXRC3_FPGA_7VX690T	
Package [1]	"FFG1761"	String indicating package type.
Flags	ADMXRC3_FPGA_SPEEDVALID	Indicates that SpeedGrade is valid; see ADMXRC3 API Specification for details of flags.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.
Stepping	""	String is empty because stepping is not defined for 7 Series FPGAs.
Present	TRUE	Should always be TRUE for normal cards.

Table 23 : Target FPGA 0 information for ADM-XRC-7V1 & ADM-VPX3-7V2

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.7 ADM-PCIE-7V3

The ADM-PCIE-7V3 has a single user-programmable FPGA with index 0, which serves both as the PCI Express host interface and the target FPGA. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 24 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of (Device String + Package String). For example, "7vx690tffg1157".
FamilyCode [1]	7 => ADMXRC3_FAMILY_7SERIES	
SubfamilyCode [1]	Varies according to device fitted: 115 => ADMXRC3_SUBFAMILY_7VXT	
PackageCode	0x46460485 => FFG1157	Numerical code indicating package type.
Device [1]	Varies according to device fitted: ° => ADMXRC3_FPGA_7VX690T	
Package	"FFG1157"	String indicating package type.

Table 24 : Target FPGA 0 information for ADM-PCIE-7V3 (continued on next page)

Member	Possible values	Comment
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices, or empty for production silicon.
Present	TRUE	

Table 24 : Target FPGA 0 information for ADM-PCIE-7V3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.8 ADM-XRC-KU1

The ADM-XRC-KU1 has a single user-programmable FPGA with index 0. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 25 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of ("xc" + Device String + "-" + Package String) [2]. For example, "xcku115-ffva1156".
FamilyCode [1]	8 => ADMXRC3_FAMILY_ULTRASCALE	
SubfamilyCode [1]	Varies according to device fitted: 128 => ADMXRC3_SUBFAMILY_UK	
PackageCode	0x4C4105ED => LA1517	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 323 => ADMXRC3_FPGA_KU060 326 => ADMXRC3_FPGA_KU115	
Package	"FLVA1517"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.

Table 25 : Target FPGA 0 information for ADM-XRC-KU1 (continued on next page)

Member	Possible values	Comment
Stepping		Empty string indicates production silicon.
Present	TRUE	

Table 25 : Target FPGA 0 information for ADM-XRC-KU1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

[2] In ADB3 Driver 1.4.16 and earlier, this is (Device String + Package String). It was changed in ADB3 Driver 1.4.17 to match the format of the string embedded in Ultrascale .bit files generated by Vivado.

5.9 ADM-PCIE-KU3

The ADM-PCIE-KU3 has a single user-programmable FPGA with index 0, which serves both as the PCI Express host interface and the target FPGA. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 26 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of ("xc" + Device String + "-" + Package String) [2]. For example, "xcku060-ffva1156".
FamilyCode [1]	8 => ADMXRC3_FAMILY_ULTRASCALE	
SubfamilyCode [1]	Varies according to device fitted: 128 => ADMXRC3_SUBFAMILY_UK	
PackageCode	0x46410484 => FA1156	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 322 => ADMXRC3_FPGA_KU040 323 => ADMXRC3_FPGA_KU060 324 => ADMXRC3_FPGA_KU075	
Package	"FFVA1156"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.
Stepping	Varies according to silicon that was available when card was manufactured.	String indicating stepping level; may be "ES2" for the earliest devices, or empty for production silicon.
Present	TRUE	

Table 26 : Target FPGA 0 information for ADM-PCIE-KU3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

[2] In ADB3 Driver 1.4.16 and earlier, this is (Device String + Package String). It was changed in ADB3 Driver 1.4.17 to match the format of the string embedded in Ultrascale .bit files generated by Vivado.

5.10 ADM-PCIE-8V3

The ADM-PCIE-8V3 has a single user-programmable FPGA with index 0, which serves both as the PCI Express host interface and the target FPGA. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 27 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of ("xc" + Device String + "-" + Package String). For example, "xcku060-ffva1156".
FamilyCode [1]	8 => ADMXRC3_FAMILY_ULTRASCALE	
SubfamilyCode [1]	Varies according to device fitted: 129 => ADMXRC3_SUBFAMILY_UV	
PackageCode	0x464305ED => FC1517	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 335 => ADMXRC3_FPGA_VU095	
Package	"FFVC1517"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.
Stepping		Empty string indicates production silicon.
Present	TRUE	

Table 27 : Target FPGA 0 information for ADM-PCIE-8V3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.11 ADM-PCIE-8K5

The ADM-PCIE-8K5 has a single user-programmable FPGA with index 0, which serves both as the PCI Express host interface and the target FPGA. Information returned in a ADMXRC3_FPGA_INFOA or ADMXRC3_FPGA_INFOW structure by ADMXRC3_GetFpgaInfoA or ADMXRC3_GetFpgaInfoW respectively is detailed in Table 28 below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of ("xc" + Device String + "-" + Package String). For example, "xcku115-flva1517".
FamilyCode [1]	8 => ADMXRC3_FAMILY_ULTRASCALE	
SubfamilyCode [1]	Varies according to device fitted: 128 => ADMXRC3_SUBFAMILY_UK	
PackageCode	0x4C4105ED => LA1517	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 326 => ADMXRC3_FPGA_KU115	
Package	"FLVA1517"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1E", "1I", "2C", "2E", "2I", "3C", "3E"	String indicating speed and temperature grade.
Stepping		Empty string indicates production silicon.
Present	TRUE	

Table 28 : Target FPGA 0 information for ADM-PCIE-8K5

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

6 Memory windows

The information in this section applies to the following API elements:

- Member **NumWindow** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- API functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx, ADMXRC3_GetWindowInfo, ADMXRC3_MapWindow and ADMXRC3_UnmapWindow.

Memory windows have indices in the range 0 to *n*-1, where *n* is the value of the member **NumWindow** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

6.1 Models with the normal set of four memory windows

The following models all feature a PCI Express to OCP Bridge for which the driver exposes four Memory Windows (each corresponding to a PCIe base address register):

- ADM-XRC-6TL
- ADM-XRC-6T1
- ADM-XRC-6TGE and ADM-XRC-6TGEL
- ADM-XRC-6T-DA1

- ADPE-XRC-6T and ADPE-XRC-6T-L
- ADM-XRC-7K1
- ADM-XRC-7V1
- ADM-VPX3-7V2
- ADM-XRC-KU1

The correspondence between Memory Windows and PCI Express Base Address Registers (BARs) is as shown in Table 29.

Window #	PCI BAR #	Size in bytes [5]	Usage
0	2 and 3 [4]	0x400000	FPGA space (prefetchable) [1, 3]
1	4 and 5 [4]	0x400000	FPGA space (non-prefetchable) [1]
2	1	0x1000	Model-specific registers [2]
3	0	0x1000	ADB3 PCI Express to OCP Bridge registers [2]

Table 29 : The normal set of four Memory Windows

Notes:

[1] Accesses to the FPGA space windows pass through the ADB3 PCI Express to OCP Bridge and terminate in the target FPGA.

[2] Accesses to the register windows terminate in the ADB3 PCI Express to OCP Bridge.

[3] Memory that is marked "prefetchable" is subject to prefetching. In other words, if something requests a read of a given number of bytes beginning at a given address, more data may be returned than requested. Additionally, the actual address at which prefetching begins may be rounded down to a power-of-2 address boundary that is lower than the original address. Prefetched data that is unused in satisfying the read request is discarded. This implies that either the FPGA designer should avoid implementing registers that have side-effects on reads, or that care should be taken to place such registers far enough apart to avoid unintended reads.

[4] The FPGA space BARs are each composed of two 32-bit BARs that are paired together to form a 64-bit BAR, as per the PCI Express specification.

[5] The sizes of the windows in the above table are accurate for the default factory-programmed Alpha Data supplied firmware, but not necessarily accurate if custom firmware is installed in a board.

Windows 0 and 1 are different views of the same thing, namely the "direct slave" channel to the FPGA. Software on the host can use either of these windows to perform CPU-initiated data transfer to and from the FPGA. If the FPGA design contains registers with side-effects on reading, then access to those registers is best performed using the non-prefetchable window (Window 1).

The sizes of windows 0 and 1 determine the addressing capacity of the "direct slave" channel, i.e. how much OCP address space the CPU can access. In default Alpha Data supplied firmware, this is 4 MiB, from 0x0 to 0x3FFFFF. There is a page register in the ADB3 PCI Express to OCP Bridge that augments the 22-bit OCP addresses generated by CPU-initiated accesses to windows 0 and 1, supplying bits 22 and above of the OCP address. As of ADMXRC3 API Specification 1.4.0, this register is currently not explicitly supported by the API, but can be still manipulated by applications via window 3. For details, please refer to the **FPGA_MASK**, **FPGA_PAGEL** and **FPGA_PAGEH** registers in the document "ADM-XRC-6T1 PCIe Bridge".

NOTE: Changing the page register affects **all** accesses to windows 0 and 1. Therefore, applications that have more than one thread accessing different 4 MiB pages in the OCP address space must implement a mechanism for ensuring that each thread does not interfere with the page register changes made by other threads.

6.2 ADM-XRC-6T-ADV8 & ADPE-XRC-6T-ADV (Target)

The ADM-XRC-6T-ADV8 brings together (a) a PCI Express to OCP Bridge core provided by Alpha Data and (b)

user-defined logic, in a single FPGA. Table 30 below lists the memory windows on these models along with how they relate to the PCI base address registers (BARs). Table 30 also applies to an ADM-XRC-6T-ADV Target device, because it strongly resembles the ADM-XRC-6T-ADV8 in terms of memory windows.

Window #	PCI BAR #	Size in bytes [5]	Usage
0	2 and 3 [4]	0x400000	FPGA space, user-definable logic (prefetchable) [1, 3]
1	4 and 5 [4]	0x400000	FPGA space, user-definable logic (non-prefetchable) [1]
2	1	0x1000	Model-specific registers [2]
3	0	0x1000	ADB3 PCI Express to OCP Bridge registers [2]

Table 30 : Memory windows in the ADM-XRC-6T-ADV8 & ADPE-XRC-6T-ADV (Target)

Notes:

[1] Accesses to the FPGA space windows pass through the ADB3 PCI Express to OCP Bridge and terminate in user-defined logic.

[2] Accesses to the register windows terminate in the ADB3 PCI Express to OCP Bridge.

[3] Memory that is marked "prefetchable" is subject to prefetching. In other words, if something requests a read of a given number of bytes beginning at a given address, more data may be returned than requested. Additionally, the actual address at which prefetching begins may be rounded down to a power-of-2 address boundary that is lower than the original address. Prefetched data that is unused in satisfying the read request is discarded. This implies that either the FPGA designer should avoid implementing registers that have side-effects on reads, or that care should be taken to place such registers far enough apart to avoid unintended reads.

[4] The FPGA space BARs are each composed of two 32-bit BARs that are paired together to form a 64-bit BAR, as per the PCI Express specification.

[5] The sizes of the windows in the above table are accurate for the default factory-programmed Alpha Data supplied PCI Express IP, but not necessarily accurate if custom firmware is installed in a board.

Windows 0 and 1 are different views of the same thing, namely the "direct slave" channel to the FPGA. Software on the host can use either of these windows to perform CPU-initiated data transfer to and from the FPGA. If the FPGA design contains registers with side-effects on reading, then access to those registers is best performed using the non-prefetchable window (Window 1).

The sizes of windows 0 and 1 determine the addressing capacity of the "direct slave" channel, i.e. how much OCP address space the CPU can access. In default Alpha Data supplied PCI Express IP, this is 4 MiB, from 0x0 to 0x3FFFFF. There is a page register in the ADB3 PCI Express to OCP Bridge that augments the 22-bit OCP addresses generated by CPU-initiated accesses to windows 0 and 1, supplying bits 22 and above of the OCP address. As of ADMXRC3 API Specification 1.4.0, this register is currently not explicitly supported by the API, but can be still manipulated by applications via window 3. For details, please refer to the **FPGA_MASK**, **FPGA_PAGEL** and **FPGA_PAGEH** registers in the document "ADM-XRC-6T1 PCIe Bridge".

NOTE: Changing the page register affects **all** accesses to windows 0 and 1. Therefore, applications that have more than one thread accessing different 4 MiB pages in the OCP address space must implement a mechanism for ensuring that each thread does not interfere with the page register changes made by other threads.

6.3 ADPE-XRC-6T-ADV Controller

ADPE-XRC-6T-ADV Controller features a PCI Express endpoint whose purpose is configuration and monitoring of the two Target devices on the board. Table 31 below lists the memory windows on these models along with how they relate to the PCI base address registers (BARs).

Window #	PCI BAR #	Size in bytes [3]	Usage
0	2 and 3 [2]	0x400000	Reserved
1	4 and 5 [2]	0x400000	Reserved
2	1	0x1000	Model-specific registers [1]
3	0	0x1000	ADB3 PCI Express to OCP Bridge registers [1]

Table 31 : Memory windows in the ADPE-XRC-6T-ADV Controller

Notes:

[1] Accesses to the register windows terminate in the PCI Express endpoint.

[2] Windows 0 and 1 are each composed of two 32-bit BARs that are paired together to form a 64-bit BAR, as per the PCI Express specification.

[3] The sizes of the windows in the above table are accurate for the default factory-programmed Alpha Data supplied firmware, but not necessarily accurate if custom firmware is installed in a board.

6.4 Datacenter cards

Datacenter cards feature a single FPGA which serves as both the PCIe Host Interface and the target FPGA. This category of reconfigurable computing cards includes the following models:

- ADM-PCIE-7V3
- ADM-PCIE-KU3
- ADM-PCIE-8V3
- ADM-PCIE-8K5

Table 32 below lists the memory windows on these models along with how they relate to the PCI base address registers (BARs). This information applies only when using Alpha Data's Board Control and Host Interface IP (ADM-PCIE-*-BCHI); it does not apply when the Xilinx PCIe Gen 3 endpoint is instantiated directly in an FPGA design.

Window #	PCI BAR #	Size in bytes [5]	Usage
0	2 and 3 [4]	See note [5] below	FPGA space, user-definable logic (prefetchable) [1, 3]
1	4 and 5 [4]	See note [5] below	FPGA space, user-definable logic (non-prefetchable) [1]
2	1	0x1000	Model-specific registers [2]
3	0	0x1000	ADB3 PCI Express to AXI4/OCP Bridge registers [2]

Table 32 : Memory windows in datacenter cards

Notes:

[1] Accesses to the FPGA space windows pass through the ADB3 PCI Express to AXI4/OCP Bridge and terminate in user-defined logic.

[2] Accesses to the register windows terminate in the ADB3 PCI Express to AXI4/OCP Bridge.

[3] Memory that is marked "prefetchable" is subject to prefetching. In other words, if something requests a read of a given number of bytes beginning at a given address, more data may be returned than requested. Additionally, the actual address at which prefetching begins may be rounded down to a power-of-2 address boundary that is lower than the original address. Prefetched data that is unused in satisfying the read request is discarded. This implies that either the FPGA designer should avoid implementing registers that have side-effects on reads, or that care should be taken to place such registers far enough apart to avoid unintended reads.

[4] The FPGA space BARs are each composed of two 32-bit BARs that are paired together to form a 64-bit BAR, as per the PCI Express specification.

[5] The size of windows 0 and 1 is determined by options in the ADM-PCIE-*-BCHI IP customization GUI.

Windows 0 and 1 are different views of the same thing, namely the "Direct Slave" channel to the FPGA. Software on the host can use either of these windows to perform CPU-initiated data transfer to and from the FPGA. If the FPGA design contains registers with side-effects on reading, then access to those registers is best performed using the non-prefetchable window (Window 1).

The sizes of windows 0 and 1 determine the addressing capacity of the "Direct Slave" channel, i.e. how much AXI4/OCP address space the CPU can access. In default Alpha Data supplied PCI Express IP, this is 4 MiB, from 0x0 to 0x3FFFFF. There is a page register in the ADB3 PCI Express to AXI4/OCP Bridge that augments the 22-bit AXI4/OCP addresses generated by CPU-initiated accesses to windows 0 and 1, supplying bits 22 and above of the AXI4/OCP address. As of ADMXRC3 API Specification 1.4.0, this register is currently not explicitly supported by the API, but can be still manipulated by applications via window 3. For details, please refer to the **FPGA_MASK**, **FPGA_PAGEL** and **FPGA_PAGEH** registers in the document "ADM-XRC-6T1 PCIe Bridge".

NOTE: Changing the page register affects **all** accesses to windows 0 and 1. Therefore, applications that have more than one thread accessing different 4 MiB pages in the OCP address space must implement a mechanism for ensuring that each thread does not interfere with the page register changes made by other threads.

7 Sensors

The information in this section applies to the following API elements:

- Member **NumSensor** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- The structures ADMXRC3_SENSOR_INFOA and ADMXRC3_SENSOR_INFOW.
- API functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx, ADMXRC3_GetSensorInfoA, ADMXRC3_GetSensorInfoW, and ADMXRC3_ReadSensor.

Sensors have indices in the range 0 to *n*-1, where *n* is the value of the member **NumSensor** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

7.1 ADM-XRC-6TL & ADM-XRC-6T1

Table 33 below lists the available sensors on these models.

Sensor #	Unit	Datatype	Description
0	V	double	1V supply rail
1	V	double	1.5V supply rail
2	V	double	1.8V supply rail
3	V	double	2.5V supply rail
4	V	double	3.3V supply rail
5	V	double	5V supply rail
6	V	double	XMC variable power rail
7	V	double	XRM I/O voltage
8	°C	double	LM87 internal temperature
9	°C	double	Target FPGA external temperature
10	°C	double	ADB3 PCI Express to OCP Bridge temperature [1]
11	V	double	ADB3 PCI Express to OCP Bridge VCCint [1]

Table 33 : Sensors on the ADM-XRC-6TL & ADM-XRC-6T1 (continued on next page)

Sensor #	Unit	Datatype	Description
12	V	double	ADB3 PCI Express to OCP Bridge VCCaux [1]

Table 33 : Sensors on the ADM-XRC-6TL & ADM-XRC-6T1

Notes:

[1] If the driver version is earlier than 1.2.0 or the firmware version is earlier than 1.4 (PCI revision 0x04), sensors 10 to 12 are not exposed by the API and **NumSensor** is 10. Otherwise, sensors 10 to 12 are exposed by the API and **NumSensor** is (at least) 13.

7.2 ADM-XRC-6TGE & ADM-XRC-6TGEL

Table 34 below lists the available sensors on the ADM-XRC-6TGE.

Sensor #	Unit	Datatype	Description
0	V	double	1V supply rail
1	V	double	1.5V supply rail
2	V	double	1.8V supply rail
3	V	double	2.5V supply rail
4	V	double	3.3V supply rail
5	V	double	5V supply rail
6	V	double	XMC variable power rail
7	V	double	XRM I/O voltage
8	°C	double	LM87 internal temperature
9	°C	double	Target FPGA external temperature
10	°C	double	ADB3 PCI Express to OCP Bridge temperature
11	V	double	ADB3 PCI Express to OCP Bridge VCCint
12	V	double	ADB3 PCI Express to OCP Bridge VCCaux

Table 34 : Sensors on the ADM-XRC-6TGE & ADM-XRC-6TGEL

7.3 ADM-XRC-6T-ADV8

Table 35 below lists the available sensors on the ADM-XRC-6T-ADV8.

Sensor #	Unit	Datatype	Description
0	V	double	3.3V supply rail
1	V	double	5V/12V XMC VPWR rail [1]
2	V	double	5V supply rail
3	V	double	1V supply rail
4	V	double	1.5V supply rail
5	V	double	1.8V supply rail
6	V	double	2.5V supply rail
7	V	double	VDD for 156.25 MHz reference oscillator

Table 35 : Sensors on the ADM-XRC-6T-ADV8 (continued on next page)

Sensor #	Unit	Datatype	Description
8	°C	double	Microcontroller internal temperature
9	°C	double	FPGA internal temperature diode
10	°C	double	Optical transceiver temperature
11	°C	double	FPGA internal temperature, from Xilinx System Monitor
12	V	double	double
13	V	double	FPGA VCCaux, from Xilinx System Monitor
14	s	double	Total 3.3VAux on time since manufacture
15		UINT32 / uint32_t	Event counter; counts power cycles

Table 35 : Sensors on the ADM-XRC-6T-ADV8

Notes:

[1] The description of sensor 1 as reported by the ADMXRC3 API was corrected in release 1.4.6 of the ADB3 Driver, across all supported platforms. In the 1.4.5 release or earlier, it is incorrectly described as "12V supply rail".

7.4 ADPE-XRC-6T & ADPE-XRC-6T-L

Table 36 below lists the available sensors on the ADPE-XRC-6T and ADPE-XRC-6T-L.

Sensor #	Unit	Datatype	Description
0	V	double	12V supply rail
1	V	double	5V supply rail
2	V	double	3.3V slot supply rail
3	V	double	3.3V internal supply rail
4	V	double	2.5V supply rail
5	V	double	FMC VADJ supply rail
6	V	double	FMC VIOB supply rail
7	V	double	1.8V supply rail
8	V	double	1.5V supply rail
9	V	double	1V supply rail
10	V	double	1V GTX supply rail
11	V	double	1.2V GTX supply rail
12	°C	double	Microcontroller internal temperature
13	°C	double	Board temperature
14	°C	double	Target FPGA temperature diode
15	°C	double	ADB3 PCI Express to OCP Bridge FPGA temperature diode
16	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature, from Xilinx System Monitor

Table 36 : Sensors on the ADPE-XRC-6T(-L) (continued on next page)

Sensor #	Unit	Datatype	Description
17	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCint, from Xilinx System Monitor
18	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCaux, from Xilinx System Monitor
19	s	double	Total powered on time since manufacture
20		UINT32 / uint32_t	Event counter; counts power cycles

Table 36 : Sensors on the ADPE-XRC-6T(-L)

7.5 ADPE-XRC-6T-ADV Controller

The sensors on the ADPE-XRC-6T-ADV can be read only via the Controller device. Table 37 below lists the available sensors on the ADPE-XRC-6T-ADV Controller.

Sensor #	Unit	Datatype	Description
0	V	double	5V supply rail
1	V	double	3.3V supply rail from PCI Express slot
2	V	double	12V supply rail
3	V	double	2.5V supply rail
4	V	double	1.8V supply rail
5	V	double	1.5V supply rail
6	V	double	1V supply rail for target FPGA 0
7	V	double	1V supply rail for target FPGA 1
8	A	double	3.3V supply rail current (from PCI Express slot)
9	A	double	12V supply current
10	°C	double	Microcontroller (system monitor) internal temperature
11	°C	double	Board temperature at target FPGA 0
12	°C	double	Board temperature at target FPGA 1
13	°C	double	Controller FPGA temperature diode
14	°C	double	Target FPGA 0 temperature diode
15	°C	double	Target FPGA 1 temperature diode
16	s	double	Total powered on time since manufacture
17		UINT32 / uint32_t	Event counter; counts power cycles

Table 37 : Sensors on the ADPE-XRC-6T-ADV Controller

7.6 ADM-XRC-7K1

Table 38 below lists the available sensors on the ADM-XRC-7K1.

Sensor #	Unit	Datatype	Description
0	V	double	5V / 12V XMC variable supply rail
1	V	double	12V XMC supply rail
2	V	double	5V XMC supply rail
3	V	double	3.3V XMC supply rail
4	V	double	2.5V supply rail
5	V	double	2V XMC auxilliary VI/O rail
6	V	double	1.8V supply rail
7	V	double	1.8V MGT AVCCaux rail
8	V	double	1.5V DDR3 SDRAM supply rail
9	V	double	XRM variable VI/O rail
10	V	double	1V supply rail
11	V	double	1.2V target FPGA AVCC rail
12	V	double	1.0V target FPGA AVCC rail
13	V	double	1.0V PCI Express to OCP Bridge FPGA AVCC rail
14	°C	double	Microcontroller (system monitor) internal temperature
15	°C	double	Board temperature measured at central point
16	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature diode
17	°C	double	Target FPGA internal temperature diode
18	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature, from Xilinx System Monitor
19	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCint, from Xilinx System Monitor
20	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCaux, from Xilinx System Monitor
21	s	double	Total powered on time since manufacture
22		UINT32 / uint32_t	Event counter; counts power cycles

Table 38 : Sensors on the ADM-XRC-7K1

7.7 ADM-XRC-7V1

Table 39 below lists the available sensors on the ADM-XRC-7V1.

Sensor #	Unit	Datatype	Description
0	V	double	5V / 12V XMC variable power rail
1	V	double	12V XMC power rail
2	V	double	5V XMC power rail
3	V	double	3.3V XMC power rail

Table 39 : Sensors on the ADM-XRC-7V1 (continued on next page)

Sensor #	Unit	Datatype	Description
4	V	double	2.5V power rail
5	V	double	2.0V Target VCCAux IO rail
6	V	double	1.8V power rail
7	V	double	1.8V Target VCCAux
8	V	double	1.8V Target MGT VCCAux
9	V	double	1.5V DDR3 SDRAM power rail
10	V	double	XRM variable VI/O rail
11	V	double	1.0V power rail
12	V	double	1.2V target MGT AVTT
13	V	double	1.0V target MGT AVCC
14	°C	double	Microcontroller (system monitor) internal temperature
15	°C	double	Board temperature measured at central point
16	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature diode
17	°C	double	Target FPGA internal temperature diode
18	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature, from Xilinx System Monitor
19	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCint, from Xilinx System Monitor
20	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCaux, from Xilinx System Monitor
21	s	double	Total powered on time since manufacture
22		UINT32 / uint32_t	Event counter; counts power cycles

Table 39 : Sensors on the ADM-XRC-7V1

7.8 ADM-VPX3-7V2

Table 40 below lists the available sensors on the ADM-VPX3-7V2.

Sensor #	Unit	Datatype	Description
0	V	double	12V VPX power rail
1	V	double	5V VPX power rail
2	V	double	3.3V VPX power rail
3	V	double	2.5V power rail
4	V	double	2.0V target VCCAux IO
5	V	double	1.8V power rail
6	V	double	1.8V target VCCAux
7	V	double	1.8V target MGT VCCAux

Table 40 : Sensors on the ADM-VPX3-7V2 (continued on next page)

Sensor #	Unit	Datatype	Description
8	V	double	1.5V DDR3 SDRAM power rail
9	V	double	FMC VADJ power rail
10	V	double	1.0V power rail
11	V	double	1.2V target MGT AVCC
12	V	double	1.0V target MGT AVCC
13	V	double	1.2V bridge MGT AVCC
14	°C	double	Microcontroller (system monitor) internal temperature
15	°C	double	Board temperature measured at central point
16	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature diode
17	°C	double	Target FPGA internal temperature diode
18	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature, from Xilinx System Monitor
19	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCint, from Xilinx System Monitor
20	V	double	ADB3 PCI Express to OCP Bridge FPGA VCCaux, from Xilinx System Monitor
21	s	double	Total powered on time since manufacture
22		UINT32 / uint32_t	Event counter; counts power cycles

Table 40 : Sensors on the ADM-VPX3-7V2

7.9 ADM-PCIE-7V3

If the ADB3 Driver version is 1.4.15 or earlier or the PCIe IP revision is 0x02 or lower, the ADMXRC3 API does not expose any sensors for the ADM-PCIE-7V3.

If the ADB3 Driver version is 1.4.16 or later and the PCIe IP revision is 0x03 or higher, the ADMXRC3 API exposes 13 sensors for the ADM-PCIE-7V3. These sensors are detailed in Table 41 below.

Sensor #	Unit	Datatype	Description
0	V	double	2.0V VCCAux IO power rail
1	V	double	1.8V MGT VCCAUx power rail
2	V	double	1.8V VCCAux power rail
3	V	double	1.2V MGT AVTT rail
4	V	double	1.0V MGT AVCC power rail
5	V	double	1.0V FPGA power rail
6	A	double	2.0V VCCAux IO current
7	A	double	1.8V MGT VCCAUx current
8	A	double	1.8V VCCAux current

Table 41 : Sensors on the ADM-PCIE-7V3 (continued on next page)

Sensor #	Unit	Datatype	Description
9	A	double	1.2V MGT AVTT current
10	A	double	1.0V MGT AVCC current
11	A	double	1.0V FPGA current
12	°C	double	FPGA internal temperature diode

Table 41 : Sensors on the ADM-PCIE-7V3

7.10 ADM-XRC-KU1

Table 42 below lists the available sensors on the ADM-XRC-KU1.

Sensor #	Unit	Datatype	Description
0	V	double	5V / 12V XMC variable power rail
1	V	double	12V XMC power rail
2	V	double	5V XMC power rail
3	V	double	3.3V XMC power rail
4	V	double	2.5V power rail
5	V	double	1.8V power rail
6	V	double	0.95V power rail
7	V	double	1.8V Bridge VCCAux
8	V	double	1.2V DDR4 SDRAM power rail
9	V	double	XRM variable VI/O rail
10	V	double	1.0V power rail
11	V	double	1.2V target MGT AVCC
12	V	double	1.0V target MGT AVCC
13	V	double	1.0V bridge MGT AVCC
14	°C	double	Microcontroller (system monitor) internal temperature
15	°C	double	Board temperature measured at central point
16	°C	double	ADB3 PCI Express to OCP Bridge FPGA internal temperature diode
17	°C	double	Target FPGA internal temperature diode
18	s	double	Total powered on time since manufacture
19		UINT32 / uint32_t	Event counter; counts power cycles

Table 42 : Sensors on the ADM-XRC-KU1

7.11 ADM-PCIE-KU3

The ADMXRC3 API exposes 13 sensors for the ADM-PCIE-KU3. These sensors are detailed in Table 43 below.

Sensor #	Unit	Datatype	Description
0	V	double	12V power rail (edge connector)
1	V	double	3.3V power rail (edge connector)
2	V	double	3.3V power rail (internal)
3	V	double	1.8V power rail
4	V	double	1.0V MGT VCCAux power rail
5	V	double	1.5V SODIMM 0 power rail
6	V	double	1.5V SODIMM 1 power rail
7	V	double	1.2V MGT AVTT
8	V	double	1.0V MGT AVCC
9	V	double	0.95V power rail
10	A	double	12V current (edge connector)
11	A	double	3.3V current (edge connector)
12	°C	double	FPGA internal temperature diode

Table 43 : Sensors on the ADM-PCIE-KU3

7.12 ADM-PCIE-8V3 & ADM-PCIE-8K5

The ADMXRC3 API exposes 18 sensors for the ADM-PCIE-8V3 & ADM-PCIE-8K5. These sensors are detailed in Table 44 below.

Sensor #	Unit	Datatype	Description
0	V	double	12V power rail (edge connector)
1	V	double	3.3V power rail (edge connector)
2	V	double	3.3VAux power rail (edge connector)
3	V	double	2.5V power rail
4	V	double	1.8V MGT power rail
5	V	double	1.2V DDR4 SDRAM power rail
6	V	double	1.2V MGT AVTT
7	V	double	1.2V MGT AVCC
8	V	double	0.95V power rail
9	V	double	0.6V DDR4 SDRAM VTT
10	A	double	12V current (edge connector)
11	A	double	3.3V current (edge connector)
12	A	double	1.8V MGT current
13	A	double	2.5V current
14	°C	double	Microcontroller (system monitor) internal temperature
15	°C	double	FPGA temperature
16	s	double	Total powered on time since manufacture

Table 44 : Sensors on the ADM-PCIE-8V3 & ADM-PCIE-8K5 (continued on next page)

Sensor #	Unit	Datatype	Description
17		UINT32 / uint32_t	Event counter; counts power cycles

Table 44 : Sensors on the ADM-PCIE-8V3 & ADM-PCIE-8K5

8 I/O module sites

The information in this section applies to the following API elements:

- Member **NumModuleSite** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- The structures ADMXRC3_MODULE_INFOA and ADMXRC3_MODULE_INFOW.
- API functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx, ADMXRC3_GetModuleInfoA and ADMXRC3_GetModuleInfoW.

I/O module sites have indices in the range 0 to *n*-1, where *n* is the value of the member **NumModuleSite** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

8.1 ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL, ADM-XRC-7K1 & ADM-XRC-7V1

The ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE, ADM-XRC-6TGEL, ADM-XRC-7K1 and ADM-XRC-7V1 each have one I/O module site with index 0, which accepts an XRM (an Alpha Data supplied I/O personality module). The values in the structure ADMXRC3_MODULE_INFOA or ADMXRC3_MODULE_INFOW depend on whether or not a module is fitted, and its type. If the module has a FRU ROM containing Vital Product Data for the module, a summary of it is reported via the various fields of ADMXRC3_MODULE_INFO or ADMXRC3_MODULE_INFO.

8.2 ADPE-XRC-6T & ADPE-XRC-6T-L

The ADPE-XRC-6T and ADPE-XRC-6T-L each have one I/O module site with index 0, which accepts a FMC (Flexible Mezzanine Card). The values in the structure ADMXRC3_MODULE_INFOA or ADMXRC3_MODULE_INFOW depend on whether or not a module is fitted, and its type. A summary of the module's FRU ROM, which contains Vital Product Data for the module, it is reported via the various fields of ADMXRC3_MODULE_INFOA or ADMXRC3_MODULE_INFOW.

8.3 ADM-VPX3-7V2

The ADM-VPX3-7V2 has one I/O module site with index 0, which accepts a FMC (Flexible Mezzanine Card). The values in the structure ADMXRC3_MODULE_INFOA or ADMXRC3_MODULE_INFOW depend on whether or not a module is fitted, and its type. A summary of the module's FRU ROM, which contains Vital Product Data for the module, it is reported via the various fields of ADMXRC3_MODULE_INFOA or ADMXRC3_MODULE_INFOW.

9 Memory banks

The information in this section applies to the following API elements:

- Members **NumMemoryBank** and **MemoryBankPresent** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- The structure ADMXRC3_BANK_INFO.
- API functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx and ADMXRC3_GetBankInfo.

Memory banks have indices in the range 0 to *n*-1, where *n* is the value of the member **NumMemoryBank** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

9.1 ADM-XRC-6TL / -6T1 / -6TGE / -6TGEL / -6T-DA1 & ADM-XRC-6T-ADV8

The ADM-XRC-6TL / -6T1 / -6TGE / -6TGEL / -6T-DA1 and ADM-XRC-6T-ADV8 can be ordered with up to four banks of either 256 MiB or 512 MiB of DDR3 SDRAM in the -187 (533 MHz) speed grade, with 32-bit physical data width per bank (as two x16 devices). Thus, **NumMemoryBank** is 4 and the total memory fitted can be 1 GiB or 2 GiB. If less than four banks are populated, some of the low four bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all four banks are populated, **MemoryBankPresent** is 0xF.

Note that not all Virtex-6 speed grades can reliably interface to DDR3 SDRAM at 533 MHz. 400 MHz is the baseline DDR3 device clock frequency for reliable operation with any Virtex-6 LXT or SXT speed grade.

Table 45 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [1, 2]	533300000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [2, 3]	0x4000000, 0x8000000	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [3]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 45 : Memory banks on ADM-XRC-6TL / -6T1 / -6TGE / -6TGEL / -6T-DA1 & ADM-XRC-6T-ADV8

Notes:

[1] Not all Virtex-6 speed grades can reliably interface to DDR3 SDRAM at 533 MHz. 400 MHz is the baseline DDR3 device clock frequency for reliable operation with any Virtex-6 LXT or SXT speed grade.

[2] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[3] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.2 ADPE-XRC-6T & ADPE-XRC-6T-L

The ADPE-XRC-6T and ADPE-XRC-6T-L accomodate up to two banks of either 256 MiB or 512 MiB of DDR3 SDRAM in the -187 (533 MHz) speed grade, with 32-bit physical data width per bank (as two x16 devices). Thus, **NumMemoryBank** is 2 and the total memory fitted can be 512 MiB or 1 GiB. If less than two banks are populated, some of the low two bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If

both banks are populated, **MemoryBankPresent** is 0x3.

Table 46 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [1, 2]	533300000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [2, 3]	0x4000000, 0x8000000	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [3]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 46 : Memory bank information for the ADPE-XRC-6T(-L)

Notes:

[1] Not all Virtex-6 speed grades can reliably interface to DDR3 SDRAM at 533 MHz. 400 MHz is the baseline DDR3 device clock frequency for reliable operation with any Virtex-6 LXT or SXT speed grade.

[2] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[3] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.3 ADPE-XRC-6T-ADV

The number of banks of memory reported by the ADMXRC3 API depends on whether ADMXRC3_GetCardInfo (Ex) is called for the Controller or for a Target device:

- From the point of view of the Controller device, the ADPE-XRC-6T-ADV has eight banks of memory in total - four per Target device. The Controller has visibility of the memory banks attached to each Target device.
- From the point of view of a Target device, there are four banks of memory, which are the memory banks connected directly to it. A Target device does not have visibility of the memory banks of the other Target device.

This arrangement is covered in detail in the next two subsections.

9.3.1 ADPE-XRC-6T-ADV Controller

When ADMXRC3_GetCardInfo (Ex) is called for the Controller device, the **NumMemoryBank** field of the returned ADMXRC3_CARD_INFO (EX) structure is 8. Banks 0 to 3 are connected directly to Target FPGA 0, and banks 4 to 7 are connected directly to Target FPGA 1. The total memory fitted can be 2 GiB or 4 GiB. If less than eight banks are populated, some of the low eight bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. For example, if banks 0, 1, 5 and 6 populated, **MemoryBankPresent** is 0x33.

When ADMXRC3_GetBankInfo is called for the Controller device, the **ConnectivityMask** field indicates to which target FPGA a memory bank is directly connected. For memory banks 0 to 3, the value is 0x1 (indicating target FPGA 0), whilst for memory banks 4 to 7, the value is 0x2 (indicating target FPGA 1). Thus, Table 47 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [1, 2]	533300000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [2, 3]	0x4000000, 0x8000000	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [3]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 (banks 0 to 3) => connected to target FPGA 0 0x2 (banks 4 to 7) => connected to target FPGA 1	bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 47 : Memory bank information for the ADPE-XRC-6T-ADV Controller

Notes:

[1] Not all Virtex-6 speed grades can reliably interface to DDR3 SDRAM at 533 MHz. 400 MHz is the baseline DDR3 device clock frequency for reliable operation with any Virtex-6 LXT or SXT speed grade.

[2] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[3] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.3.2 ADPE-XRC-6T-ADV Target

When ADMXRC3_GetCardInfo (Ex) is called for a Target device, the **NumMemoryBank** field of the returned ADMXRC3_CARD_INFO (EX) structure is 4, and the total memory fitted (for that Target device) can be 1 GiB or 2 GiB. If less than four banks are populated, some of the low four bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all four banks are populated, **MemoryBankPresent** is 0xF.

Table 48 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [1, 2]	533300000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [2, 3]	0x4000000, 0x8000000	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [3]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Connected to self	bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 48 : Memory bank information for an ADPE-XRC-6T-ADV Target

Notes:

[1] Not all Virtex-6 speed grades can reliably interface to DDR3 SDRAM at 533 MHz. 400 MHz is the baseline DDR3 device clock frequency for reliable operation with any Virtex-6 LXT or SXT speed grade.

[2] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[3] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.4 ADM-XRC-7K1

The ADM-XRC-7K1 accomodates up to two banks of either 256 MiB or 512 MiB of DDR3 SDRAM in the -125 (800 MHz) speed grade, with 16-bit physical data width per bank (as one x16 device). Thus, **NumMemoryBank** is 2 and the total memory fitted can be 512 MiB or 1 GiB. If less than two banks are populated, some of the low two bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If both banks are populated, **MemoryBankPresent** is 0x3.

Table 49 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [2]	800000000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [2]	0x8000000, 0x10000000	Number of memory words in the bank.
PhysicalDataWidth	16	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.

Table 49 : Memory banks on ADM-XRC-7K1 (continued on next page)

Member	Possible values	Comment
PhysicalWidth [2]	16	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 49 : Memory banks on ADM-XRC-7K1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.5 ADM-XRC-7V1 & ADM-VPX3-7V2

The ADM-XRC-7V1 and ADM-VPX3-7V2 accomodate up to four banks of 256 MiB, 512 MiB or 1 GiB of DDR3 SDRAM in the -125 (800 MHz) speed grade, with 32-bit physical data width per bank (as two x16 devices). Thus, **NumMemoryBank** is 4 and the total memory fitted can be 1 GiB, 2 GiB or 4 GiB. If less than four banks are populated, some of the low four bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all banks are populated, **MemoryBankPresent** is 0xF.

Table 50 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [2]	800000000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [2]	0x4000000, 0x8000000, 0x10000000	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [2]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 50 : Memory banks on ADM-XRC-7V1 & ADM-VPX3-7V2

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.6 ADM-PCIE-7V3

The ADM-PCIE-7V3 has two DDR3 SODIMM slots, each of which can accommodate a 4 GiB or 8 GiB SODIMM. The ADB3 Driver uses the Serial Presence Detect (SPD) PROM on each SODIMM in order to present a summary of the SODIMM's information in the ADMXRC3_BANK_INFO structure. This means that the values returned in each field depend upon the contents of the SPD PROM. Nevertheless, some values are fixed, and possible values are indicated in Table 51:

Member	Possible values	Comment
MaximumFrequency [2, 3]	666666667 800000000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [1, 2]	0x20000000 => 4 GiB 0x40000000 => 8 GiB	Number of physical memory words in the bank.
PhysicalDataWidth	64	Number of bits in a physical memory word.
PhysicalECCWidth	0 => No ECC 8 => ECC present	Indicates whether or not SODIMM has ECC bits.
PhysicalWidth [2]	64 or 72	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 51 : Memory banks on ADM-PCIE-7V3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger or faster speed grades of SODIMMs. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

[3] Actual **MaximumFrequency** values returned in the structure may differ slightly from the possible values presented here because they must be calculated from information in the SODIMM's SPD PROM, and are thus subject to rounding errors.

9.7 ADM-XRC-KU1

The ADM-XRC-KU1 accomodate up to four banks of 2 GiB of DDR4 SDRAM in the -083E (1200 MHz) speed grade, with 32-bit physical data width per bank (as two x16 devices). Thus, **NumMemoryBank** is 4 and the total memory fitted is up to 8 GiB. If less than four banks are populated, some of the low four bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all banks are populated, **MemoryBankPresent** is 0xF.

Table 52 below details the information returned by ADMXRC3_GetBankInfo in the ADMXRC3_BANK_INFO structure:

Member	Possible values	Comment
MaximumFrequency [2]	1200000000	Hz
MinimumFrequency	625000000	Hz
PhysicalSize [2]	0x20000000 => 2 GiB	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [2]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x100 => ADMXRC3_BANK_SDRAM_DDR4	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 52 : Memory banks on ADM-XRC-KU1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger sizes or faster speed grades of DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.8 ADM-PCIE-KU3

The ADM-PCIE-KU3 has two DDR3 SODIMM slots, each of which can accommodate a 4 GiB or 8 GiB SODIMM. The ADB3 Driver uses the Serial Presence Detect (SPD) PROM on each SODIMM in order to present a summary of the SODIMM's information in the ADMXRC3_BANK_INFO structure. This means that the values returned in each field depend upon the contents of the SPD PROM. Nevertheless, some values are fixed, and possible values are indicated in Table 53:

Member	Possible values	Comment
MaximumFrequency [2, 3]	666666667 800000000	Hz
MinimumFrequency	303030303	Hz
PhysicalSize [1, 2]	0x20000000 => 4 GiB 0x40000000 => 8 GiB	Number of physical memory words in the bank.
PhysicalDataWidth	64	Number of bits in a physical memory word.
PhysicalECCWidth	8 => ECC present	Indicates whether or not SODIMM has ECC bits.

Table 53 : Memory banks on ADM-PCIE-KU3 (continued on next page)

Member	Possible values	Comment
PhysicalWidth [2]	72	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 53 : Memory banks on ADM-PCIE-KU3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger or faster speed grades of SODIMMs. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

[3] Actual **MaximumFrequency** values returned in the structure may differ slightly from the possible values presented here because they must be calculated from information in the SODIMM's SPD PROM, and are thus subject to rounding errors.

9.9 ADM-PCIE-8V3

The ADM-PCIE-8V3 has two banks of 72-bit wide DDR4 SDRAM, each made up of nine 8-bit wide components in the -083E (1200 MHz) speed grade. As of writing, 8 GiB per bank is the only available memory option, but in future it is expected that a 16 GiB (per bank) option will be made available. If less than two banks are populated, some of the low two bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all banks are populated, **MemoryBankPresent** is 0x3.

Member	Possible values	Comment
MaximumFrequency [2, 3]	1200000000	Hz
MinimumFrequency	625000000	Hz
PhysicalSize [1, 2]	0x40000000 => 8 GiB 0x80000000 => 16 GiB	Number of physical memory words in the bank.
PhysicalDataWidth	64	Number of bits in a physical memory word.
PhysicalECCWidth	8 => ECC present	Indicates whether or not SODIMM has ECC bits.
PhysicalWidth [2]	72	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x100 => ADMXRC3_BANK_SDRAM_DDR4	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.

Table 54 : Memory banks on ADM-PCIE-8V3 (continued on next page)

Member	Possible values	Comment
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 54 : Memory banks on ADM-PCIE-8V3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger or faster speed grades of SODIMMs. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

9.10 ADM-PCIE-8K5

The ADM-PCIE-8K5 has two banks of 72-bit wide DDR4 SDRAM, each made up of nine 8-bit wide components in the -083E (1200 MHz) speed grade. As of writing, 8 GiB per bank is the only available memory option, but in future it is expected that a 16 GiB (per bank) option will be made available. If less than two banks are populated, some of the low two bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all banks are populated, **MemoryBankPresent** is 0x3.

Member	Possible values	Comment
MaximumFrequency [2, 3]	1200000000	Hz
MinimumFrequency	625000000	Hz
PhysicalSize [1, 2]	0x40000000 => 8 GiB 0x80000000 => 16 GiB	Number of physical memory words in the bank.
PhysicalDataWidth	64	Number of bits in a physical memory word.
PhysicalECCWidth	8 => ECC present	Indicates whether or not SODIMM has ECC bits.
PhysicalWidth [2]	72	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x100 => ADMXRC3_BANK_SDRAM_DDR4	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 55 : Memory banks on ADM-PCIE-8K5

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit larger or faster speed grades of SODIMMs. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

10 Flash memory banks

The information in this section applies to the following API elements:

- Member **NumFlashBank** of structures ADMXRC3_CARD_INFO and ADMXRC3_CARD_INFOEX.
- The structures ADMXRC3_FLASH_INFOA and ADMXRC3_FLASH_INFOW.
- API functions ADMXRC3_GetCardInfo, ADMXRC3_GetCardInfoEx, ADMXRC3_GetFlashInfoA and ADMXRC3_GetFlashInfoW.

Flash memory banks have indices in the range 0 to *n*-1, where *n* is the value of the member **NumFlashBank** of the structure ADMXRC3_CARD_INFO (EX) returned by ADMXRC3_GetCardInfo (Ex).

10.1 ADM-XRC-6TL / -6T1 / -6TGE / -6T-DA1 / -7K1 / -7V1 & ADPE-XRC-6T(-L)

The ADM-XRC-6TL / -6T1 / -6TGE / -6T-DA1 / -7K1 and ADPE-XRC-6T(-L) each have a single bank of Flash memory with index 0 that is guaranteed to be at least 64 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 56 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000	Size of user-programmable area, in bytes.

Table 56 : Flash bank 0 on ADM-XRC-6TL / -6T1 / -6TGE / -6TGEL / -6T-DA1 / -7K1 / -7V1 & ADPE-XRC-6T(-L)

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a different Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 57 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	VPD space address [2]	Usage
0x0000000 - 0x07FFFFF	N/A	Alternate ADB3 PCIe to OCP Bridge bitstream [1]
0x0800000 - 0x0FFFFFF	N/A	Default ADB3 PCIe to OCP Bridge bitstream [1]
0x1000000 - 0x10FFFFF	0x000000 - 0x0FFFFF	Alpha Data VPD region [3, 5]

Table 57 : Flash bank 0 address map for ADM-XRC-6TL / -6T1 / -6TGE / -6TGEL / -6T-DA1 / -7K1 / -7V1 & ADPE-XRC-6T(-L) (continued on next page)

Flash byte address	VPD space address [2]	Usage
0x1100000 - 0x11FFFFF	0x100000 - 0x1FFFFF	Customer VPD region (user-programmable) [4, 5]
0x1200000 - 0x28FFFFF	N/A	Region 0 [6] Target FPGA default bitstream (user-programmable)
0x2900000 - 0x3FFFFFF	N/A	Region 1 [7] Target FPGA failsafe bitstream (user-programmable)

Table 57 : Flash bank 0 address map for ADM-XRC-6TL / -6T1 / -6TGE / -6TGEL / -6T-DA1 / -7K1 / -7V1 & ADPE-XRC-6T(-L)

Notes:

[1] The Alternate and Default ADB3 PCIe to OCP Bridge bitstream areas are not user-programmable, and the ADMXRC3 API does not provide functions that can access them, in order to prevent accidental corruption. Only a firmware update can write to these areas.

[2] VPD space is the address space used by the API functions ADMXRC3_ReadVPD and ADMXRC3_WriteVPD.

[3] Alpha Data programs this region with Vital Product Data (VPD) at manufacture-time.

[4] Guaranteed not to be used for anything by Alpha Data. Any application-specific information can be stored here.

[5] As a precaution against accidental writes, the Alpha Data supplied driver does not permit writes to this region unless a failsafe mechanism is disabled; refer to the release notes for the ADB3 driver for details.

[6] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND certain switches are set appropriately. Refer to the user guide for the model in question for details of the available switches.

[7] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND at least one of the following conditions holds:

(a) Configuration from the "Target FPGA bitstream" area is disabled via switches.

(b) The "Target FPGA bitstream" area is blank.

(c) The "Target FPGA bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

In effect, this area stores a failsafe bitstream that is used if configuration with the "Target FPGA bitstream" cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. This is a precautionary measure against Negative Bias Temperature Instability (NBTI) effects.

NOTE
Alpha Data recommends that region 1 (**Target FPGA failsafe bitstream**) is never erased. If overwritten, it must be written with a bitstream that is valid for the target FPGA. Otherwise, the protection conferred by the factory-programmed bitstream against Negative Bias Temperature Instability (NBTI) effects will be removed.

10.2 ADM-XRC-6T-ADV8

The ADM-XRC-6T-ADV8 has a single bank of Flash memory with index 0 that is guaranteed to be at least 64 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 58 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000	Size of user-programmable area, in bytes.

Table 58 : Flash bank 0 information for the ADM-XRC-6T-ADV8

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a different Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 59 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0000000 - 0x1FFFFFF	Region 0 [2] Failsafe FPGA bitstream (user-programmable)
0x2000000 - 0x3FFFFFF	Region 1 [1] Default FPGA bitstream (user-programmable)

Table 59 : Flash bank 0 address map for the ADM-XRC-6T-ADV8

Notes:

[1] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up.

[2] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up, provided that at least one of the following conditions holds:

(a) The "Default FPGA bitstream" area is blank.

(b) The "Default FPGA bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

In effect, this area stores a failsafe bitstream that is used if configuration with the "Default FPGA bitstream" cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. This is a precautionary measure against Negative Bias Temperature Instability (NBTI) effects.

NOTE
Alpha Data recommends that region 0 (**FPGA failsafe bitstream**) is never erased. If overwritten, it must be written with a bitstream that is valid for the target FPGA. Otherwise, the protection conferred by the factory-programmed bitstream against Negative Bias Temperature Instability (NBTI) effects will be removed.

10.3 ADPE-XRC-6T-ADV Controller

The ADPE-XRC-6T-ADV Controller has two banks of Flash memory for storing FPGA bitstreams for the two Target devices on the board. Each Flash bank is guaranteed to be at least 64 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 60 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000	Size of user-programmable area, in bytes.

Table 60 : Flash bank 0 / 1 information for the ADPE-XRC-6T-ADV Controller

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a different Flash memory device is fitted.

[3] This value is guaranteed not to change.

From the Controller's point of view, Flash memory bank 0 pertains to Target device 0, which equates to target FPGA 0. Similarly Flash memory bank 1 pertains to Target device 1, which equates to target FPGA 1. From the point of view of a Target device, there is no visibility of the Flash memory bank that holds its bitstreams. In others, all programming of bitstreams for a Target device **must** be performed via the Controller.

Flash memory bank 0 also contains the firmware for the Controller itself.

Table 61 and Table 62 below show the address maps, which are guaranteed not to change, for the two Flash memory banks:

Flash byte address	Usage
0x0000000 - 0x07FFFFF	Alternate Controller bitstream [1]
0x8000000 - 0x0FFFFFF	Default Controller bitstream [1]
0x1000000 - 0x10FFFFF	Reserved
0x1100000 - 0x11FFFFF	Customer region (user-programmable) [2]
0x1200000 - 0x28FFFFF	Region 0 [3] Target FPGA 0 default bitstream (user-programmable)
0x2900000 - 0x3FFFFFF	Region 1 [4] Target FPGA 0 failsafe bitstream (user-programmable)

Table 61 : Flash bank 0 address map for the ADPE-XRC-6T-ADV Controller

Flash byte address	Usage
0x0000000 - 0x10FFFFF	Reserved
0x1100000 - 0x11FFFFF	Customer region (user-programmable) [2]
0x1200000 - 0x28FFFFF	Region 0 [3] Target FPGA 1 default bitstream (user-programmable)

Table 62 : Flash bank 1 address map for the ADPE-XRC-6T-ADV Controller (continued on next page)

Flash byte address	Usage
0x2900000 - 0x3FFFFFF	Region 1 [4] Target FPGA 1 failsafe bitstream (user-programmable)

Table 62 : Flash bank 1 address map for the ADPE-XRC-6T-ADV Controller

Notes:

[1] The Alternate and Default Controller bitstream areas are not user-programmable, and the ADMXRC3 API does not provide functions that can access them, in order to prevent accidental corruption. Only a firmware update can write to these areas.

[2] Guaranteed not to be used for anything by Alpha Data. Any application-specific information can be stored here.

[3] The Controller will attempt to configure target FPGA *n* with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND certain switches are set appropriately. Refer to the user guide for the model in question for details of the available switches.

[4] The Controller will attempt to configure target FPGA *n* with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND at least one of the following conditions holds:

(a) Configuration from the "Target FPGA *n* bitstream" area is disabled via switches.

(b) The "Target FPGA *n* bitstream" area is blank.

(c) The "Target FPGA *n* bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

In effect, this area stores a failsafe bitstream that is used if configuration from the "Target FPGA *n* bitstream" area cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. This is a precautionary measure against Negative Bias Temperature Instability (NBTI) effects.

NOTE
Alpha Data recommends that region 1 (**Target FPGA *n* failsafe bitstream**) of either Flash bank is never erased. If overwritten, it must be written with a bitstream that is valid for the target FPGA. Otherwise, the protection conferred by the factory-programmed bitstream against Negative Bias Temperature Instability (NBTI) effects will be removed.

10.4 ADM-XRC-7K1 / -7V1

The ADM-XRC-7K1 / -7V1 each have a single bank of Flash memory with index 0 that is guaranteed to be at least 64 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 63 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000	Size of user-programmable area, in bytes.

Table 63 : Flash bank 0 on ADM-XRC-7K1 / -7V1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a different Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 64 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0000000 - 0x07FFFFF	Alternate ADB3 PCIe to OCP Bridge bitstream [1]
0x0800000 - 0x0FFFFFF	Default ADB3 PCIe to OCP Bridge bitstream [1]
0x1000000 - 0x11FFFFF	Reserved
0x1200000 - 0x28FFFFF	Region 0 [2] Target FPGA default bitstream (user-programmable)
0x2900000 - 0x3FFFFFF	Region 1 [3] Target FPGA failsafe bitstream (user-programmable)

Table 64 : Flash bank 0 address map for ADM-XRC-7K1 / -7V1

Notes:

[1] The Alternate and Default ADB3 PCIe to OCP Bridge bitstream areas are not user-programmable, and the ADMXRC3 API does not provide functions that can access them, in order to prevent accidental corruption. Only a firmware update can write to these areas.

[2] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND certain switches are set appropriately. Refer to the user guide for the model in question for details of the available switches.

[3] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND at least one of the following conditions holds:

(a) Configuration from the "Target FPGA bitstream" area is disabled via switches.

(b) The "Target FPGA bitstream" area is blank.

(c) The "Target FPGA bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

In effect, this area stores a failsafe bitstream that is used if configuration with the "Target FPGA bitstream" cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. However, 7 Series FPGAs are not known to be susceptible to Negative Bias Temperature Instability (NBTI) effects, so this is a merely precautionary measure.

10.5 ADM-VPX3-7V2

The ADM-VPX3-7V2 has a single bank of Flash memory with index 0 whose size is guaranteed to be at least 64 MiB or 128 MiB, depending on the target FPGA device that is fitted:

- For the 7V585T, 7VX330T, 7VX415T and 7VX485T the minimum size is 64 MiB.
- For the 7V2000T, 7VX585T, 7VX690T, 7VX980T, 7VX1140T, 7VH580T and 7VH870T the minimum size is 128 MiB.

Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 65 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000, 0x8000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000, 0x6E00000	Size of user-programmable area, in bytes.

Table 65 : Flash bank 0 on ADM-VPX3-7V2

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is sufficiently large to accomodate normal and failsafe bitstreams for the target FPGA device that is fitted. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a different Flash memory device is fitted.

[3] This value is guaranteed not to change.

The address map for Flash bank 0 depends upon its size. In effect, the user-programmable area of Flash bank 0 is divided into two equally-sized regions, with the first allocated to the normal Target FPGA 0 bitstream, and the second dedicated to the failsafe Target FPGA 0 bitstream. This arrangement is shown in Table 66 for a 64 MiB bank and in Table 67 for a 128 MiB bank:

Flash byte address	Usage
0x0000000 - 0x07FFFFF	Alternate ADB3 PCIe to OCP Bridge bitstream [1]
0x0800000 - 0x0FFFFFF	Default ADB3 PCIe to OCP Bridge bitstream [1]
0x1000000 - 0x11FFFFF	Reserved
0x1200000 - 0x28FFFFF	Region 0 [2] Target FPGA default bitstream (user-programmable)
0x2900000 - 0x3FFFFFF	Region 1 [3] Target FPGA failsafe bitstream (user-programmable)

Table 66 : 64 MiB Flash bank 0 address map for ADM-VPX3-7V2

Flash byte address	Usage
0x0000000 - 0x07FFFFF	Alternate ADB3 PCIe to OCP Bridge bitstream [1]
0x0800000 - 0x0FFFFFF	Default ADB3 PCIe to OCP Bridge bitstream [1]
0x1000000 - 0x11FFFFF	Reserved
0x1200000 - 0x48FFFFF	Region 0 [2] Target FPGA default bitstream (user-programmable)
0x4900000 - 0x7FFFFFF	Region 1 [3] Target FPGA failsafe bitstream (user-programmable)

Table 67 : 128 MiB Flash bank 0 address map for ADM-VPX3-7V2

Notes:

[1] The Alternate and Default ADB3 PCIe to OCP Bridge bitstream areas are not user-programmable, and the ADMXRC3 API does not provide functions that can access them, in order to prevent accidental corruption. Only a firmware update can write to these areas.

[2] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND certain switches are set appropriately. Refer to the user guide for the model in question for details of the available switches.

[3] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND at least one of the following conditions holds:

(a) Configuration from the "Target FPGA bitstream" area is disabled via switches.

(b) The "Target FPGA bitstream" area is blank.

(c) The "Target FPGA bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

In effect, this area stores a failsafe bitstream that is used if configuration with the "Target FPGA bitstream" cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. However, 7 Series FPGAs are not known to be susceptible to Negative Bias Temperature Instability (NBTI) effects, so this is a merely precautionary measure.

10.6 ADM-PCIE-7V3

The ADM-PCIE-7V3 board revision 2 has a Micron MT28GU01GAAA1E Flash device (known as G18 for short). This Flash device is used to configure the FPGA on the ADM-PCIE-7V3 in BPI mode at the fastest possible speed.

Table 68 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Micron MT28GU01GAAA1E"	String indicating what Flash memory device is fitted.
Size [2]	0x8000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x8000000	Size of user-programmable area, in bytes.

Table 68 : Flash bank 0 information for the ADM-PCIE-7V3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 128 MiB and the Flash device is fully compatible with the G18 Flash device, such that FPGA bitstreams do not need to be regenerated for the new Flash device. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a larger Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 69 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0000000 - 0x1FFFFFF	Region 0 - Target FPGA failsafe bitstream (user-programmable)
0x2000000 - 0x3FFFFFF	Region 1 - Target FPGA default bitstream (user-programmable)

Table 69 : Flash bank 0 address map for the ADM-PCIE-7V3 (continued on next page)

Flash byte address	Usage
0x4000000 - 0x5FFFFFF	Region 2 - User-definable (user-programmable)
0x6000000 - 0x7FFFFFF	Region 3 - User-definable (user-programmable)

Table 69 : Flash bank 0 address map for the ADM-PCIE-7V3

At power-on, the ADM-PCIE-7V3 initially attempts to configure the FPGA in BPI mode from one of the above four regions. The region used depends upon switch settings, which control pullup / pulldown resistors connected to the upper two Flash address lines. For full details, refer to the **ADM-PCIE-7V3 User Manual**, but the information is reproduced here for convenience:

SW1-1	SW1-3	Flash region used for power-on configuration
OFF	OFF	Region 0
OFF	ON	Region 1 (factory default)
ON	OFF	Region 2
ON	ON	Region 3

Table 70 : Switch settings affecting configuration from Flash on ADM-PCIE-7V3

If power-on configuration fails, the FPGA may (depending on bitstream options) fall back to configuring from another region, where the FPGA overrides the pullup / pulldown resistors. For full details, refer to **Xilinx UG470, "7 Series FPGAs Configuration"**.

10.7 ADM-XRC-KU1

The ADM-XRC-KU1 has a single bank of Flash memory with index 0 that is guaranteed to be at least 128 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 71 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x8000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x6E00000	Size of user-programmable area, in bytes.

Table 71 : Flash bank 0 on ADM-XRC-KU1

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a different Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 72 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0000000 - 0x07FFFFF	Alternate ADB3 PCIe to OCP Bridge bitstream [1]
0x0800000 - 0x0FFFFFF	Default ADB3 PCIe to OCP Bridge bitstream [1]
0x1000000 - 0x11FFFFF	Reserved
0x1200000 - 0x4FFFFFF	Target FPGA bitstream (user-programmable) [2]
0x5000000 - 0x7FFFFFF	Available for user data (user-programmable) [3]

Table 72 : Flash bank 0 address map for ADM-XRC-KU1

Notes:

[1] The Alternate and Default ADB3 PCIe to OCP Bridge bitstream areas are not user-programmable, and the ADMXRC3 API does not provide functions that can access them, in order to prevent accidental corruption. Only a firmware update can write to these areas.

[2] Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND switch SW1-4 is OFF. Refer to the user guide for the ADM-XRC-KU1 in question for details of the switch settings.

[3] Any user-defined data can be stored in this region.

10.8 ADM-PCIE-KU3

The ADM-PCIE-KU3 (board revision 2 and later) has a Micron MT28GU01GAAA1E Flash device (known as G18 for short). This Flash device is used to configure the FPGA on the ADM-PCIE-KU3 in BPI mode at the fastest possible speed.

Table 73 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Micron MT28GU01GAAA1E"	String indicating what Flash memory device is fitted.
Size [2]	0x8000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x8000000	Size of user-programmable area, in bytes.

Table 73 : Flash bank 0 information for the ADM-PCIE-KU3

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 128 MiB and the Flash device is fully compatible with the G18 Flash device, such that FPGA bitstreams do not need to be regenerated for the new Flash device. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a larger Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 74 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0000000 - 0x1FFFFFF	Region 0 - Target FPGA failsafe bitstream (user-programmable)
0x2000000 - 0x3FFFFFF	Region 1 - Target FPGA default bitstream (user-programmable)
0x4000000 - 0x5FFFFFF	Region 2 - User-definable (user-programmable)
0x6000000 - 0x7FFFFFF	Region 3 - User-definable (user-programmable)

Table 74 : Flash bank 0 address map for the ADM-PCIE-KU3

At power-on, the ADM-PCIE-KU3 initially attempts to configure the FPGA in BPI mode from one of the above four regions. The region used depends upon switch settings, which control pullup / pulldown resistors connected to the upper two Flash address lines. For full details, refer to the **ADM-PCIE-KU3 User Manual**, but the information is reproduced here for convenience:

SW1-3	SW1-4	Flash region used for power-on configuration
OFF	OFF	Region 0
OFF	ON	Region 1 (factory default)
ON	OFF	Region 2
ON	ON	Region 3

Table 75 : Switch settings affecting configuration from Flash on ADM-PCIE-KU3

If power-on configuration fails, the FPGA may (depending on bitstream options) fall back to configuring from another region, where the FPGA overrides the pullup / pulldown resistors. For full details, refer to **Xilinx UG570, "Ultrascale Architecture Configuration"**.

10.9 ADM-PCIE-8V3 & ADM-PCIE-8K5

The ADM-PCIE-8V3 & ADM-PCIE-8K5 have a Micron MT28GU01GAAA1E Flash device (known as G18 for short). This Flash device is used to configure the FPGA in BPI mode at the fastest possible speed.

Table 76 shows the information returned by ADMXRC3_GetFlashInfoA or ADMXRC3_GetFlashInfoW:

Member	Possible values	Comment
Identifier [1]	"Micron MT28GU01GAAA1E"	String indicating what Flash memory device is fitted.
Size [2]	0x8000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x8000000	Size of user-programmable area, in bytes.

Table 76 : Flash bank 0 information for the ADM-PCIE-8V3/-8K5

Notes:

[1] Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 128 MiB and the Flash device is fully compatible with the G18 Flash device, such that FPGA bitstreams do not need to be regenerated for the new Flash device. This may be unavoidable if, for example, a particular device reaches end-of-life.

[2] Minimum value; may be larger if a larger Flash memory device is fitted.

[3] This value is guaranteed not to change.

Table 77 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0000000 - 0x3FFFFFF	Region 0 - Available for user data / bitstreams (user-programmable)
0x4000000 - 0x7FFFFFF	Region 1 - Target FPGA default bitstream (user-programmable)

Table 77 : Flash bank 0 address map for the ADM-PCIE-8V3/-8K5

At power-on, the ADM-PCIE-8V3/-8K5 attempts to configure the FPGA in BPI mode from region 1. Region 0 can be used to store an alternate bitstream (e.g. for IPROG reconfiguration or fallback) or any user-defined data.

Revision History

Date	Revision	Nature of Change
28/02/2011	1.0	Initial version
24/06/2011	1.1	Added information for ADM-XRC-6TGE. Corrected frequency range of ADM-XRC-6TL clock generator 0.
19/09/2011	1.2	Added information for ADM-XRC-6T-ADV8.
14/05/2012	1.3	Corrected PCI subsystem device ID for ADM-XRC-6T-ADV8 Updated sensor 1 description returned by driver for ADM-XRC-6T-ADV8. Moved memory window information for ADM-XRC-6T-ADV8 into a separate section. Added information for ADPE-XRC-6T and ADPE-XRC-6T-L. Added preliminary information for ADPE-XRC-6T-ADV. Added preliminary information for ADM-XRC-7K1.
16/07/2012	1.4	Added information for ADM-XRC-6T-DA1. Added information for ADM-XRC-7V1. Information for ADPE-XRC-6T(-L) and ADM-XRC-7K1 is no longer preliminary.
25/07/2013	1.5	Added information for ADM-XRC-6TGEL. Added information for ADM-VPX3-7V2. Corrected PCIe to OCP Bridge clock synthesizer pins for ADM-XRC-7K1 in Section 3.6. Added (+) and (-) for clock pins to show differential pairs in Section 3. Corrected incorrect family code number in Section 5.5 and Section 5.6.
27/03/2014	1.6	Added datatypes of sensor values to tables that detail available sensors for each board. Corrected description of "Time since manufacture" sensor for all models to read "Total powered on time since manufacture" for all models except ADM-XRC-6T-ADV8. Corrected description of "Time since manufacture" sensor of ADM-XRC-6T-ADV8 to read "Total 3.3VAux on time since manufacture".
08/08/2014	1.7	Added information for ADM-PCIE-7V3.
02/03/2015	1.8	Added information for ADM-PCIE-KU3. Added information for the ADM-PCIE-7V3's clock generators and sensors. Corrected "FPGA FPGA temperature diode" throughout document to read "FPGA internal temperature diode". Changed "SW1A" & "SW1C" to "SW1-1" & "SW1-3" to better match information in ADM-PCIE-7V3 User Manual. Added extended temperature range SpeedGrade possibilities to FPGA information for 7 Series models.
06/03/2015	1.9	Labelled the regions of Flash memory that can be used for FPGA configuration

Date	Revision	Nature of Change
6th May 2016	1.10	Corrected description of string format of Identifier member of ADMXRC3_FPGA_INFO{A,W} structure. Corrected IOSTANDARD for SODIMM reference clocks of ADM-PCIE-KU3. Corrected PhysicalDataWidth value for ADM-PCIE-KU3. Added information about ADM-XRC-KU1. Added information about ADM-PCIE-8V3. Added information about ADM-PCIE-8K5.

Address: 4 West Silvermills Lane, Edinburgh, EH3 5BD, UK
Telephone: +44 131 558 2600
Fax: +44 131 558 2700
email: sales@alpha-data.com
website: http://www.alpha-data.com

Address: 3507 Ringsby Court Suite 105, Denver, CO 80216
Telephone: (303) 954 8768
Fax: (866) 820 9956 toll free
email: sales@alpha-data.com
website: http://www.alpha-data.com