ALPHA DATA

ADM-XRC-KU1 Support & Development Kit Release: 0.1.0

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1 Introduction

The **ADM-XRC-KU1 Support & Development Kit (SDK)** is a set of resources for FPGA designers and software engineers working with Alpha Data's ADM-XRC-KU1 reconfigurable computing card.

The resources of the ADM-XRC-KU1 SDK include:

- Resources for developing application software for a machine that hosts Alpha Data reconfigurable computing hardware:
  - C/C++ header files and libraries which provide Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Documentation about Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Common utilities (with source code) for viewing information about reconfigurable computing devices, programming nonvolatile memory, and more.
- Example FPGA designs and host programs (with source code) demonstrating various features of the ADM-XRC-KU1:
  - The **Standalone DDR4 Test FPGA Design** demonstrates how to use the onboard DDR4 SDRAM memories.
  - The **DMA Demonstration FPGA Design** demonstrates how to use the DMA channels (AXI4) of Alpha Data's **ADM-XRC-KU1-HSAXI** IP in order to transfer between the target FPGA and the host, via the PCIe to MPTL Bridge.
  - The **DMA Demonstration (PCIe) FPGA Design** demonstrates the use of Alpha Data's **ADM-XRC-KU1-P5HI** IP, which includes a PCI Express endpoint with DMA engines (AXI4).
  - The **Simple Demonstration FPGA Design** contains a more or less minimal set of logic, including **ADM-XRC-KU1-HSAXI**, that enables the host CPU to read and write register in the target FPGA, via the PCIe to MPTL Bridge.
  - The **Simple Demonstration (OCP) FPGA Design** is functionally similar to **Simple Demonstration FPGA Design**, but uses OCP protocol and the **ADM-XRC-KU1-HSOCP** IP. It is provided in order to ease migration from Alpha Data's earlier reconfigurable computing products.
- IP and common HDL code for the target FPGA, provided by Alpha Data:
  - **ADM-XRC-KU1-HSAXI** Host Interface IP, which provides an MPTL to AXI4 interface with DMA channels, as well as other features. This allows the host CPU to exchange data with the target FPGA via the PCIe to MPTL Bridge.
  - **ADM-XRC-KU1-HSOCP** Host Interface IP, which provides an MPTL to OCP interface with DMA channels, as well as other features. This IP performs a similar function to **ADM-XRC-KU1-HSAXI**, but with OCP protocol rather than AXI4, and is provided in order to ease migration from Alpha Data's earlier reconfigurable computing products.
  - **ADM-XRC-KU1-P5HI** PCIe Host Interface IP, which provides a PCI Express to AXI4 interface with a configurable number of DMA engines (AXI4), as well as other features, in the target FPGA. This is provided for applications which transfer data to the target FPGA whilst bypassing the PCIe to MPTL Bridge.
  - Common HDL code (i.e. not specific to the ADM-XRC-KU1), used by the example FPGA designs.

1.1 Structure of this package

The directories making up the ADM-XRC-KU1 SDK are organised as in Figure 1 below:

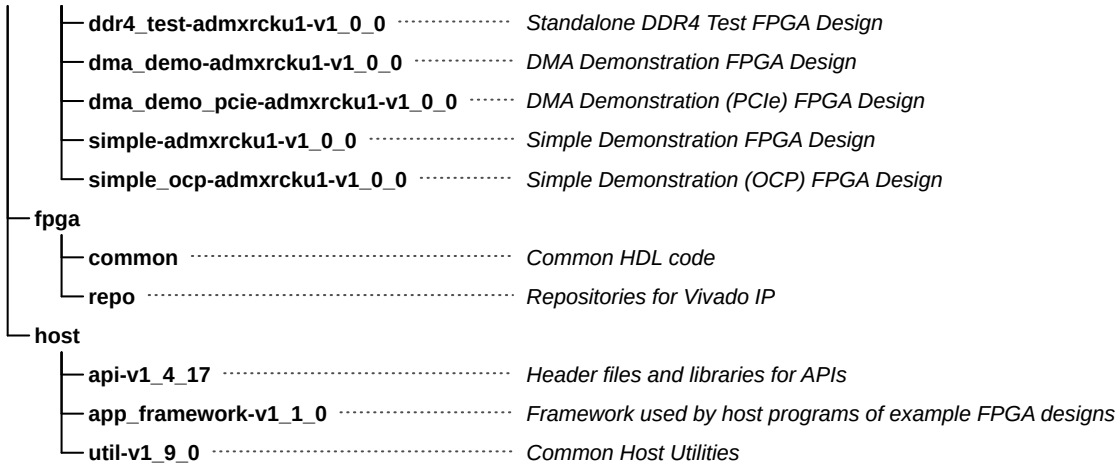

Figure 1 : Structure of the SDK

2 Development operating system support

2.1 Windows

Generally speaking, Alpha Data's Windows software, when supplied in binary form, is compatible with Windows XP and later. However, the choice of Windows operating system used for development mainly depends upon which releases of Microsoft Visual Studio and/or Xilinx Vivado are chosen for a project.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore a Windows operating system must be capable of running Vivado. As of writing, Vivado 2016.2 is the current release, and Windows 7, Windows 8.1 and Windows 10 are recommended.

Vivado path length issue
In Windows, Vivado requires that path lengths of files are no greater than the **MAX_PATH** Win32 constant, which is 260 characters (including the NUL character used to terminate a string). This limit is easily exceeded when a Vivado project uses IP (cores) and the path length of the Vivado project file (.xpr) exceeds about 80 characters. Exceeding the **MAX_PATH** limit can result in otherwise inexplicable failures when implementing an FPGA design in Vivado.

The recommended workaround for this issue is to use the **subst** command to map a drive letter (e.g. **Z:**) to the root of this SDK. If done correctly, the result is the existence of directories **Z:\doc**, **Z:\example**, **Z:\fpga** etc.

When developing software to run on a host machine, Microsoft Visual Studio is likely to be used for building applications. Therefore, the Windows operating system must be capable of running a particular version of Microsoft Visual Studio. For Microsoft Visual Studio 2012 or 2013, Windows 7, Windows 8.1 and Windows 10 are recommended.

2.2 Linux

Alpha Data generally does not supply binaries for Linux because of the large number of architectures and configurations that exist across various Linux distributions. Source code is provided, however, and can be built for most Linux distributions.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore the supported Linux distributions depend upon the release of Vivado chosen for a project. As of writing, Vivado 2016.2 is the current release and therefore the following Linux distributions are recommended:

- Red Hat Enterprise Workstation 5.11, 6.6 - 6.7 & 7.0 - 7.1 (64-bit)
- CentOS 6.7 & 7.1 (64-bit)
- SUSE Linux Enterprise 11.3 & 12.0 (64-bit)
- Ubuntu Linux 14.04 LTS (64-bit)

Linux distributions that are not listed might result in Vivado failing to work, or only partially working. They are not supported by Xilinx.

3 Associated documents

(1) Common Host Utilities
(root)/host/util-v1_9_0/doc/ad-ug-0055_v1_1.pdf

(2) ADMXRC3 API Specification
(root)/host/api-v1_4_17/doc/ad-ug-0003_v1_13.pdf

(3) ADMXRC3 API Hardware Addendum
(root)/host/api-v1_4_17/doc/ad-ug-0009_v1_10.pdf

(4) ADM-XRC-KU1 Standalone DDR4 Test FPGA Design
(root)/ddr4_test-admxrcku1-v1_0_0/doc/ad-ug-0058_v1_0.pdf

(5) Using Xilinx Ultrascale MIG with the ADM-XRC-KU1
(root)/ddr4_test-admxrcku1-v1_0_0/doc/ad-ug-0059_v1_0.pdf

(6) ADM-XRC-KU1 DMA Demonstration FPGA Design
(root)/dma_demo-admxrcku1-v1_0_0/doc/ad-ug-0067_v1_0.pdf

(7) ADM-XRC-KU1 DMA Demonstration (PCIe) FPGA Design
(root)/dma_demo_pcie-admxrcku1-v1_0_0/doc/ad-ug-0069_v1_0.pdf

(8) ADM-XRC-KU1 Simple Demonstration FPGA Design
(root)/simple-admxrcku1-v1_0_0/doc/ad-ug-0060_v1_0.pdf

(9) ADM-XRC-KU1 Simple Demonstration (OCP) FPGA Design
(root)/simple_ocp-admxrcku1-v1_0_0/doc/ad-ug-0079_v1_0.pdf

4 Release history

4.1 Release 1.0.0

This is the first release of the ADM-XRC-KU1 Support & Development Kit.

Revision History

Date	Revision	Nature of change
21 Jul 2016	1.0	Initial version.

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