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ADM-XRC Gen 3
SDK 1.5.0 Patch 2
Release Note

Introduction

This Release Note describes the "ADM-XRC Gen 3 SDK 1.5.0 Patch 2 (ADM-XRC-7K1 and ADM-XRC-7V1 Production Silicon)".

> **Note**
> In order to support production silicon Kintex-7 and Virtex-7 devices found on the latest ADM-XRC-7K1 and ADM-XRC-7V1 XMC boards, the ADM-XRC Gen 3 SDK 1.5.0 requires this patch.

This patch consists of a collection of files that overwrite those found in the ADM-XRC Gen 3 SDK 1.5.0, which only supports Initial Engineering Silicon Kintex-7 and Virtex-7 devices.

Supported operating systems

This SDK supports the following operating systems:

*   Windows NT-based operating systems beginning with Windows 2000. Both 32-bit and 64-bit editions are supported.
*   Linux distributions running a 2.6.x or 3.x.y kernel.

Beginning with release 1.2.0, this SDK includes header files and example code for VxWorks. For VxWorks development, it is assumed that a host / development machine is available that runs one of the above operating systems.

Supported Alpha Data hardware

The example applications and HDL code in this patch support the following models in Alpha Data's range of reconfigurable computing hardware:

*   ADM-XRC-7K1 with production silicon
*   ADM-XRC-7V1 with production silicon

Supported Silicon Revisions

Unpatched, the ADM-XRC Gen 3 SDK 1.5.0 only has support for Kintex-7 and Virtex-7 Initial Engineering Silicon.

After this patch is applied, the ADM-XRC Gen SDK 1.5.0 will only support Kintex-7 and Virtex-7 Production Silicon.

Differences

Notable differences between the unpatched ADM-XRC Gen 3 SDK 1.5.0 SDK and the patched version are described in the following sections.

Kintex-7 Production Silicon FPGA Development

This section supersedes section 5.2.2 of the SDK user guide.

In this patched version of the SDK, for Kintex-7 FPGAs, Production Silicon is supported. These devices are marked with a blank SCD code, whereas devices with Initial Engineering Silicon are marked with the SCD code "ES9937".

Xilinx ISE 14.4 or later is recommended, together with the following patches:

- MIG 7 Series v1.8 DDR2/DDR3 Calibration Update patch (Xilinx Answer 53420). This patch consists of a set of Verilog files that must be copied into the MIG7 v1.8 HDL source folder for the ADM-XRC-7K1 **AFTER** generating the core, overwriting whatever files were generated. This is described further in the file **hdl/vhdl/common/ddr3_sdram_if/admxrc7v1/mig7_v1_8/tactical_patch_ar53420.txt**.

Bitstreams targeting 7K325T and 7K410T production devices must be generated in ISE 14.2 or later versions of the design tools (Xilinx Answer 50906).

Note: The MIG7 series v1.8 DDR3 interface used by default by this version of the SDK is only supported by ISE 14.4 and above. It is the first production standard MIG7 version and Alpha Data recommends its use.

Virtex-7 Production Silicon FPGA Development

This section supersedes section 5.2.3 of the SDK user guide.

In this patched version of the SDK, for Virtex-7 FPGAs, Production Silicon is supported. These devices are marked with a blank SCD code, whereas devices with Initial Engineering Silicon are marked with the SCD code "ES9937".

Xilinx ISE 14.5 is recommended, together with the following patches:

- MIG 7 Series v1.8 DDR2/DDR3 Calibration Update patch (Xilinx Answer 53420). This patch consists of a set of Verilog files that must be copied into the MIG7 v1.8 HDL source folder for the ADM-XRC-7V1 **AFTER** generating the core, overwriting whatever files were generated. This is described further in the file **hdl/vhdl/common/ddr3_sdram_if/admxrc7v1/mig7_v1_8/tactical_patch_ar53420.txt**.

Bitstreams targeting 7VX485T production devices must be generated in ISE 14.2 or later versions of the design tools (Xilinx Answer 50906).

Bitstreams targeting 7VX690T production devices must be generated in ISE 14.5 or later versions of the design tools (Xilinx Answer 50906).

Note: The MIG7 series v1.8 DDR3 interface used by default by this version of the SDK is only supported by ISE 14.4 and above. It is a production standard MIG7 version and Alpha Data recommends its use.

Bitstream Building Using Xilinx ISE

Information in this section supersedes Kintex-7 and Virtex-7 information contained in section 5.4 of the SDK user guide.

Kintex-7 Series Models

Xilinx ISE version 14.4 or later is recommended for rebuilding the Kintex-7 bitstreams for the example FPGA designs in this SDK. Refer to Section 5.2.2 - "Kintex-7 Production Silicon FPGA Development" for information about recommended Xilinx ISE versions for this release of the SDK.

Virtex-7 Series Models

Xilinx ISE version 14.5 or later is recommended for rebuilding the Virtex-7 bitstreams for the example FPGA designs in this SDK. Refer to Section 5.2.3 - "Virtex-7 Production Silicon FPGA Development" for information about recommended Xilinx ISE versions for this release of the SDK.

Bitstream Design Bitstreams Using PlanAhead

Information in this section supersedes Kintex-7 information contained in section 5.4.2 of the SDK user guide.

Kintex-7 Series Models

Xilinx ISE version 14.4 or later is recommended for rebuilding the Kintex-7 bitstreams for the example FPGA designs in this SDK. Refer to Section 5.2.2 - "Kintex-7 Production Silicon FPGA Development" for information about recommended Xilinx ISE versions for this release of the SDK.

Virtex-7 Series Models

Xilinx ISE version 14.5 or later is recommended for rebuilding the Virtex-7 bitstreams for the example FPGA designs in this SDK. Refer to Section 5.2.3 - "Virtex-7 Production Silicon FPGA Development" for information about recommended Xilinx ISE versions for this release of the SDK.

DDR3 SDRAM MIG Cores

Information in this section supersedes Kintex-7 and Virtex-7 information contained in section 6.5.1 of the SDK user guide.

MIG Version	ISE Versions
MIG7 v1.8	ISE 14.4.

Table 1 : DDR3 SDRAM MIG Core And ISE Version Compatibility

> **Note**
> This version of the SDK uses MIG7 v1.8 DDR3 SDRAM MIG cores for Kintex-7 and Virtex-7 model simulation and synthesis.

The files for each supported core version are generated using a different TCL generation script. Table 2 lists the scripts available:

MIG Version	Generation Script
MIG7 v1.8	%ADMXRC3_SDK%/hdl/vhdl/common/ddr3_sdram_if/gen_ddr3_if_mig7_v1_8.tcl

Table 2 : DDR3 SDRAM MIG core generation scripts

Examples are as follows:

To generate MIG7 v1.8 HDL files for an ADM-XRC-7K1 using Windows, start a shell and issue the following commands:

```
cd /d %ADMXRC3_SDK%\hdl\vhdl\common\ddr3_sdram_if
xtclsh gen_ddr3_if_mig7_v1_8.tcl admxrc7k1
```

To generate MIG7 v1.8 HDL files for an ADM-XRC-7K1 using Linux, start a shell and issue the following commands:

```
cd $ADMXRC3_SDK/hdl/vhdl/common/ddr3_sdram_if
xtclsh ./gen_ddr3_if_mig7_v1_8.tcl admxrc7k1
```

Xilinx documentation is included with the generated Xilinx DDR3 SDRAM MIG core. For example, after generation of the MIG7 v1.8 core for ADM-XRC-7K1 models, its documentation can be found in **hdl/vhdl/common/ddr3_sdram_if/admxrc7k1/mig7_v1_8/mig_temp/mig_v1_8/docs/**.

Similarly its VHDL source files can be found in **hdl/vhdl/common/ddr3_sdram_if/admxrc7k1/mig7_v1_8/rtl/mig_v1_8/**.

> **Note**
> The TCL script is run using the Xilinx customized TCL distribution TCL shell xtclsh. The path to this shell must be defined for successful script execution.

Installation

Installation in Windows

The ADM-XRC Gen 3 SDK 1.5.0 should be installed before applying the patch.

The **admxrcg3-sdk-win32-1.5.0_patch2.zip** file should be extracted over the top level of the existing SDK.

The user should allow existing files to be overwritten when prompted.

Installation in Linux

The ADM-XRC Gen 3 SDK 1.5.0 should be installed before applying the patch.

The **admxrcg3-sdk-linux-1.5.0_patch2.tar.gz** file should be extracted over the top level of the existing SDK. For example, if the ADM-XRC Gen 3 SDK for Linux had previously been installed so that its top level directory is **/opt/admxrcg3sdk-1.5.0**, use the following commands:

```
$ cd /opt
$ tar xzf path/to/../admxrcg3-sdk-linux-1.5.0_patch2.tar.gz
```

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Revision History

Date	Revision	Nature of Change
2 May 2013	1.0	Initial version