ALPHA DATA

ADMXRC3 API Hardware Addendum

Revision: 1.2
Date: 19th September 2011

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1 Introduction

This document accompanies the ADMXRC3 API Specification 1.4.0. This document provides information for application developers about how the hardware features of Gen 3 reconfigurable computing hardware are exposed via the ADMXRC3 API. In particular, it:

- Describes how hardware features are exposed via the ADMXRC3 API.
- Details hardware features that can be relied upon for all cards of the same model.
- Details hardware features that cannot be relied upon; for example, the end-of-life of a component may force new boards to be populated with a different, but compatible device.

The information in this document applies to the following models:

- ADM-XRC-6TL
- ADM-XRC-6T1
- ADM-XRC-6TGE
- ADM-XRC-6T-ADV8 (board revision 2 and later)

1.1 Summary of hardware features

Table 1 below summarizes models currently supported by the ADMXRC3 API:

Feature	ADM-XRC-6TL	ADM-XRC-6T1	ADM-XRC-6TGE	ADM-XRC-6T-ADV8
Host interface	PCI Express Gen 1 x4 [1]	PCI Express Gen 1/2 x4 [1]		PCI Express Gen 1/2 x4/x8 [1, 4]
PCI vendor ID	0x4144			
PCI device ID	0xADB3			
PCI subsystem vendor ID	0x4144			
PCI subsystem device ID	0x0201	0x0300	0x0301	0x0302
Model code	**0x101**	**0x102**	**0x103**	**0x104**
Number of **programmable clock generators**	**1**	**0 or 1**	**3**	0
Number of **DMA engines** [2]	**2**	**4**		**variable**
Number of **target FPGAs**	1 x Virtex-6			
Number of **memory windows**	4			
Number of **sensors** [3]	**10 or 13**		**13**	**16**
Number of **I/O module sites**	1			0
Number of **memory banks**	4			
Number of **Flash memory banks**	1			

Table 1: Summary of hardware features, by model

Notes:

1. ADB3 PCI Express to OCP Bridge, implemented in a Xilinx FPGA.
2. The number of DMA engines is permitted to increase with future firmware and/or driver updates; the values given here are minimum values.

3. The number of sensors is permitted to increase with future firmware and/or driver updates; the values given here are minimum values. To maintain compatibility with existing software, the ordering of previously existing sensors is not permitted to change.
4. The ADM-XRC-6T-ADV8 has a user-programmable Virtex-6 FPGA which serves both as the PCI Express host interface and the target FPGA for user applications. Hence, its PCI Express capabilities (Gen 1 vs. Gen 2, x4 vs. x8 etc.) are user-definable.

2 Model codes

2.1 ADM-XRC-6TL

The **Model** member of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)** has the value 0x101 (ADMXRC3_MODEL_ADMXRC6TL).

2.2 ADM-XRC-6T1

The **Model** member of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)** has the value 0x102 (ADMXRC3_MODEL_ADMXRC6T1).

2.3 ADM-XRC-6TGE

The **Model** member of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)** has the value 0x103 (ADMXRC3_MODEL_ADMXRC6TGE).

2.4 ADM-XRC-6T-ADV8

The **Model** member of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)** has the value 0x104 (ADMXRC3_MODEL_ADMXRC6TADV8).

3 Programmble clock generators

The information in this section applies to the following API elements:

- Member **NumClockGen** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- Information functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx**.
- Clock management functions **ADMXRC3_GetClockFrequency** and **ADMXRC3_SetClockFrequency**.

Programmable clock generators, if present, have indices in the range 0 to *n*-1, where *n* is the value of the member **NumClockGen** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

3.1 ADM-XRC-6TL

The ADM-XRC-6TL has a single programmable clock with index 0, named LCLK (for historical reasons), generated by a clock synthesizer in the PCI-E to OCP Bridge. Its I/O standard is LVCMOS25 and is input on pin **AY14** of the target FPGA. The frequency range of this clock is 32 MHz to 140 MHz.

3.2 ADM-XRC-6T1

If the firmware revision lower than 1.6 (PCI revision 0x06), no clock generators are available.

If the firmware revision is 1.6 (PCI revision 0x06) or higher, and the driver version is 1.3.0 or higher, the ADMXRC3 API exposes a clock generator, implemented in the PCI-E to OCP Bridge, as index 0. Its frequency range is 5 MHz to 700 MHz, and is an LVDS25 pair connected to target FPGA pins AA31 and AB31.

3.3 ADM-XRC-6TGE

The ADM-XRC-6TGE exposes 3 clock generators, as in **Table 2** below:

Index	I/O standard	Target FPGA pin(s)	Range (MHz)	Description
0	LVDS25	AA31 and AB31	5 - 700	Clock synthesizer in PCI-E to OCP Bridge
1	LVDS25	M8 and M7	5 - 312.5	SI5338 clock output 1
2	LVDS25	AF8 and AF7	5 - 312.5	SI5338 clock output 2

Table 2: ADM-XRC-6TGE clock generators

4 DMA engines

The information in this section applies to the following API elements:

- Member **NumDmaChannel** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- Information functions **ADMXRC3_GetCardInfo** and **ADMXRC3_GetCardInfoEx**.
- DMA functions **ADMXRC3_ReadDMA**, **ADMXRC3_ReadDMAEx**, **ADMXRC3_ReadDMALocked**, **ADMXRC3_ReadDMALockedEx**, **ADMXRC3_WriteDMA**, **ADMXRC3_WriteDMAEx**, **ADMXRC3_WriteDMALocked** and **ADMXRC3_WriteDMALockedEx**.
- Non-blocking DMA functions **ADMXRC3_StartReadDMA**, **ADMXRC3_StartReadDMAEx**, **ADMXRC3_StartReadDMALocked**, **ADMXRC3_StartReadDMALockedEx**, **ADMXRC3_StartWriteDMA**, **ADMXRC3_StartWriteDMAEx**, **ADMXRC3_StartWriteDMALocked** and **ADMXRC3_StartWriteDMALockedEx** and **ADMXRC3_FinishDMA**.

4.1 ADM-XRC-6TL

The ADM-XRC-6TL has 2 DMA engines, which are fully independent of one another.

In firmware **before** version 1.4 (PCI revision 0x04), the low 32 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine an addressing capacity of 4 GiB.

In firmware version 1.4 (PCI revision 0x04) and later, (at a minimum) the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of at least 512 GiB.

4.2 ADM-XRC-6T1 & ADM-XRC-6TGE

The ADM-XRC-6T1 and ADM-XRC-6TGE each have 4 DMA engines, which are fully independent of one another. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

4.3 ADM-XRC-6T-ADV8

The ADM-XRC-6T-ADV8 has up to 4 DMA engines, which are fully independent of one another. At a minimum, the low 39 bits of addresses passed in the **localAddress** parameter of the above DMA API functions are used by the hardware, with the remaining bits ignored. This gives each DMA engine a minimum addressing capacity of 512 GiB.

Since the ADM-XRC-6T-ADV8 has a single Virtex-6 FPGA that serves both as the host interface and the target FPGA for user designs, each DMA engine consumes logic resources that might otherwise be used by the user application FPGA design. Alpha Data supplies default PCI Express IP to be embedded within a user FPGA design for the ADM-XRC-6T-ADV8 that in effect has 1.5 DMA engines:

- DMA engine 0 functions normally, and transfers data in either direction (FPGA to host and host to FPGA).
- DMA engine 1 transfers data only in the FPGA to host direction, saving some logic resources in the FPGA.

Alpha Data can supply PCI Express IP with a different DMA engine configuration on request.

5 Target FPGAs

The information in this section applies to the following API elements:

- Member **NumTargetFpga** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- The structures **ADMXRC3_FPGA_INFOA** and **ADMXRC3_FPGA_INFOW**.
- Informational functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx**, **ADMXRC3_GetFpgaInfoA** and **ADMXRC3_GetFpgaInfoW**.
- Target FPGA management functions **ADMXRC3_ConfigureFromBuffer**, **ADMXRC3_ConfigureFromFileA**, **ADMXRC3_ConfigureFromFileW** and **ADMXRC3_Unconfigure**.

Target FPGAs have indices in the range 0 to *n*-1, where *n* is the value of the member **NumTargetFpga** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

5.1 ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE

The ADM-XRC-6TL, ADM-XRC-6T1 and ADM-XRC-6TGE all have a single target FPGA with index 0. Information returned in a **ADMXRC3_FPGA_INFO[A|W]** structure by **ADMXRC3_GetFpgaInfo(A|W}** is detailed in **Table 3** below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of "xc" + Device + Package + "-" + SpeedGrade + Stepping.
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1759	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 173 => ADMXRC3_FPGA_6VLX550T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1759"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 3: Target FPGA 0 information for ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE

Notes:

1. Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

5.2 ADM-XRC-6T-ADV8

The ADM-XRC-6T-ADV8 has a single user-programmable FPGA with index 0, which serves both as the PCI Express host interface and the target FPGA. Information returned in a **ADMXRC3_FPGA_INFO[A|W]** structure by **ADMXRC3_GetFpgaInfo(A|W**} is detailed in **Table 4** below:

Member	Possible values	Comment
Identifier	Varies according to device fitted.	String composed of lower-case version of "xc" + Device + Package + "-" + SpeedGrade + Stepping.
FamilyCode [1]	6 => ADMXRC3_FAMILY_VIRTEX6	
SubfamilyCode [1]	Varies according to device fitted: 98 => ADMXRC3_SUBFAMILY_6LXT 99 => ADMXRC3_SUBFAMILY_6SXT	
PackageCode	0x464606DF => FF1759	Numerical code indicating package type.
Device [1]	Varies according to device fitted: 171 => ADMXRC3_FPGA_6VLX240T 172 => ADMXRC3_FPGA_6VLX365T 173 => ADMXRC3_FPGA_6VLX550T 176 => ADMXRC3_FPGA_6VSX315T 177 => ADMXRC3_FPGA_6VSX475T	
Package	"FF1759"	String indicating package type.
Flags	Depends on driver version and Vital Product Data (VPD) version in the card. However, the flag ADMXRC3_FPGA_NOTCONFIGURABLE is always be present.	Flags that indicate if SpeedGrade and Stepping are valid; see ADMXRC3 API Specification for details.
SpeedGrade [1]	Varies according to device fitted: "1C", "1I", "2C", "2I", "3C"	String indicating speed and temperature grade.
Stepping	Varies according to when card was manufactured.	String indicating stepping level; may be "ES" for the earliest devices.
Present	TRUE	Should always be TRUE for normal cards.

Table 4: Target FPGA 0 information for ADM-XRC-6T-ADV8

Notes:

1. Not necessarily an exhaustive list; Alpha Data reserves the right to fit other devices if requested by customers.

6 Memory windows

The information in this section applies to the following API elements:

- Member **NumWindow** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- API functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx**, **ADMXRC3_GetWindowInfo**, **ADMXRC3_MapWindow** and **ADMXRC3_UnmapWindow**.

Memory windows have indices in the range 0 to *n*-1, where *n* is the value of the member **NumWindow** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

6.1 ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE & ADM-XRC-6T-ADV8

The ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE and ADM-XRC-6T-ADV8 feature a PCI Express to OCP Bridge. **Table 5** below lists the memory windows on these models along with how they relate to the PCI base address registers (BARs).

Window #	PCI BAR #	Size in bytes [5]	Usage
0	2 and 3	0x400000	FPGA space (prefetchable) [1, 3, 4]
1	4 and 5	0x400000	FPGA space (non-prefetchable) [1, 4]
2	1	0x1000	Model-specific registers [2]
3	0	0x1000	ADB3 PCI Express to OCP Bridge registers [2]

Table 5: Memory windows in the ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE & ADM-XRC-6T-ADV8

Notes:

1. Accesses to the FPGA space windows pass through the ADB3 PCI Express to OCP Bridge and terminate in the target FPGA.
2. Accesses to the register windows terminate in the ADB3 PCI Express to OCP Bridge.
3. Memory that is marked "prefetchable" is subject to prefetching. In other words, if something requests a read of a given number of bytes beginning at a given address, more data may be returned than requested. Additionally, the actual address at which prefetching begins may be rounded down to a power-of-2 address boundary that is lower than the original address. Prefetched data that is unused in satisfying the read request is discarded. This implies that either the FPGA designer should avoid implementing registers that have side-effects on reads, or that care should be taken to place such registers far enough apart to avoid unintended reads.
4. The FPGA space BARs are each composed of two 32-bit BARs that are paired together to form a 64-bit BAR, as per the PCI Express specification.
5. The sizes of the windows in the above table are accurate for the default factory-programmed Alpha Data supplied firmware, but not necessarily accurate if custom firmware is installed in a board.

Windows 0 and 1 are different views of the same thing, namely the "direct slave" channel to the FPGA. Software on the host can use either of these windows to perform CPU-initiated data transfer to and from the FPGA. If the FPGA design contains registers with side-effects on reading, then access to those registers is best performed using the non-prefetchable window (Window 1).

The sizes of windows 0 and 1 determine the addressing capacity of the "direct slave" channel, i.e. how much OCP address space the CPU can access. In default Alpha Data supplied firmware, this is 4 MiB, from 0x0 to 0x3FFFFF. There is a page register in the ADB3 PCI Express to OCP Bridge that augments the 22-bit OCP addresses generated by CPU-initiated accesses to windows 0 and 1, supplying bits 22 and above of the OCP address. As of ADMXRC3 API Specification 1.4.0, this register is currently not explicitly supported by the API, but can be still manipulated by applications via window 3. For details, please refer to the **FPGA_MASK**, **FPGA_PAGEL** and **FPGA_PAGEH** registers in the document "ADM-XRC-6T1 PCI-E Bridge".

NOTE: Changing the page register affects **all** accesses to windows 0 and 1. Therefore, applications that have more than one thread accessing different 4 MiB pages in the OCP address space must implement a mechanism for ensuring that each thread does not interfere with the page register changes made by other threads.

7 Sensors

The information in this section applies to the following API elements:

- Member **NumSensor** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- The structures **ADMXRC3_SENSOR_INFOA** and **ADMXRC3_SENSOR_INFOW**.
- API functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx**, **ADMXRC3_GetSensorInfoA**, **ADMXRC3_GetSensorInfoW**, and **ADMXRC3_ReadSensor**.

Sensors have indices in the range 0 to *n*-1, where *n* is the value of the member **NumSensor** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

7.1 ADM-XRC-6TL & ADM-XRC-6T1

Table 6 below lists the available sensors on these models.

Sensor #	Unit	Description
0	V	1V supply rail
1	V	1.5V supply rail
2	V	1.8V supply rail
3	V	2.5V supply rail
4	V	3.3V supply rail
5	V	5V supply rail
6	V	XMC variable power rail
7	V	XRM I/O voltage
8	°C	LM87 internal temperature
9	°C	Target FPGA external temperature
10	°C	ADB3 PCI Express to OCP Bridge temperature [1]
11	V	ADB3 PCI Express to OCP Bridge VCCINT [1]
12	V	ADB3 PCI Express to OCP Bridge VCCAUX [1]

Table 6: Sensors in the ADM-XRC-6TL & ADM-XRC-6T1

Notes:

1. If the driver version is earlier than 1.2.0 or the firmware version is earlier than 1.4 (PCI revision 0x04), sensors 10 to 12 are not exposed by the API and **NumSensor** is 10. Otherwise, sensors 10 to 12 are exposed by the API and **NumSensor** is (at least) 13.

7.2 ADM-XRC-6TGE

Table 7 below lists the available sensors on the ADM-XRC-6TGE.

Sensor #	Unit	Description
0	V	1V supply rail
1	V	1.5V supply rail
2	V	1.8V supply rail
3	V	2.5V supply rail
4	V	3.3V supply rail
5	V	5V supply rail
6	V	XMC variable power rail
7	V	XRM I/O voltage
8	°C	LM87 internal temperature
9	°C	Target FPGA external temperature
10	°C	ADB3 PCI Express to OCP Bridge temperature
11	V	ADB3 PCI Express to OCP Bridge VCCINT
12	V	ADB3 PCI Express to OCP Bridge VCCAUX

Table 7: Sensors in the ADM-XRC-6TGE

7.3 ADM-XRC-6T-ADV8

Table 8 below lists the available sensors on the ADM-XRC-6T-ADV8.

Sensor #	Unit	Description
0	V	3.3V supply rail
1	V	12V supply rail
2	V	5V supply rail
3	V	1V supply rail
4	V	1.5V supply rail
5	V	1.8V supply rail
6	V	2.5V supply rail
7	V	VDD for 156.25 MHz reference oscillator
8	°C	Microcontroller internal temperature
9	°C	FPGA internal temperature diode
10	°C	Optical transceiver temperature
11	°C	FPGA internal temperature from Xilinx System Monitor
12	V	FPGA VCCInt
13	V	FPGA VCCAux
14	s	Time since manufacture
15		Event counter; counts power cycles

Table 8: Sensors in the ADM-XRC-6T-ADV8

8 I/O module sites

The information in this section applies to the following API elements:

- Member **NumModuleSite** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- The structures **ADMXRC3_MODULE_INFOA** and **ADMXRC3_MODULE_INFOW**.
- API functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx**, **ADMXRC3_ModuleInfoA** and **ADMXRC3_ModuleInfoW**.

I/O module sites have indices in the range 0 to *n*-1, where *n* is the value of the member **NumModuleSite** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

8.1 ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE

The ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE each have one I/O module site with index 0. The values in the structure **ADMXRC3_MODULE_INFO(A|W)** depend on whether or not a module is fitted, and its type. If the module has a FRU ROM containing Vital Product Data for the module, it is reported via the various fields of **ADMXRC3_MODULE_INFO(A|W)**.

9 Memory banks

The information in this section applies to the following API elements:

- Members **NumMemoryBank** and **MemoryBankPresent** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- The structure **ADMXRC3_BANK_INFO**.
- API functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx** and **ADMXRC3_GetBankInfo**.

Memory banks have indices in the range 0 to *n*-1, where *n* is the value of the member **NumMemoryBank** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

9.1 ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE & ADM-XRC-6T-ADV8

The ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE and ADM-XRC-6T-ADV8 can be ordered with up to four banks of either 256 MiB or 512 MiB of DDR3 SDRAM in the -187 (533 MHz) speed grade, with 32-bit physical data width per bank (as two x16 devices). Thus, **NumMemoryBank** is 4 and the total memory fitted can be 1 GiB or 2 GiB. If less than four banks are populated, some of the low four bits of **MemoryBankPresent** are 0, indicating which banks are unpopulated. If all four banks are populated, **MemoryBankPresent** is 0xF.

Note that not all Virtex-6 speed grades can reliably interface to DDR3 SDRAM at 533 MHz. 400 MHz is the baseline DDR3 device clock frequency for reliable operation with any Virtex-6 LXT or SXT speed grade.

Table 9 below details the information returned by **ADMXRC3_GetBankInfo** in the **ADMXRC3_BANK_INFO** structure:

Member	Possible values	Comment
MaximumFrequency [1]	533300000	
MinimumFrequency	303030303	
PhysicalSize [1, 2]	0x4000000, 0x8000000	Number of memory words in the bank.
PhysicalDataWidth	32	Number of bits in a memory word.
PhysicalECCWidth	0	No ECC bits.
PhysicalWidth [2]	32	Sum of PhysicalDataWidth and PhysicalECCWidth.
TypeMask	0x80 => ADMXRC3_BANK_SDRAM_DDR3	Indicates the type of memory in the bank.
ConnectivityMask	0x1 => Target FPGA 0	Bitmask indicating which target FPGAs are connected to the bank.
Present	TRUE, FALSE	TRUE => bank is populated and the other members are valid. FALSE => bank is unpopulated and none of the other members are valid.

Table 9: Memory bank information for the ADM-XRC-6TL, ADM-XRC-6T1, ADM-XRC-6TGE & ADM-XRC-6T-ADV8

Notes:

1. Not necessarily an exhaustive list; Alpha Data reserves the right to fit other DDR3 SDRAM devices. This may be unavoidable if, for example, a particular device reaches end-of-life.
2. Multiplying **PhysicalSize** and **PhysicalWidth** together gives the capacity of the memory bank, in bits.

10 Flash memory banks

The information in this section applies to the following API elements:

- Member **NumFlashBank** of structures **ADMXRC3_CARD_INFO** and **ADMXRC3_CARD_INFOEX**.
- The structures **ADMXRC3_FLASH_INFOA** and **ADMXRC3_FLASH_INFOW**.
- API functions **ADMXRC3_GetCardInfo**, **ADMXRC3_GetCardInfoEx**, **ADMXRC3_GetFlashInfoA** and **ADMXRC3_GetFlashInfoW**.

Flash memory banks have indices in the range 0 to *n*-1, where *n* is the value of the member **NumFlashBank** of the structure **ADMXRC3_CARD_INFO(EX)** returned by **ADMXRC3_GetCardInfo(Ex)**.

10.1 ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE

The ADM-XRC-6TL, ADM-XRC-6T1 and ADM-XRC-6TGE have a single bank of Flash memory with index 0 that is guaranteed to be at least 64 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 10 shows the information returned by **ADMXRC3_GetFlashInfo(A|W)**:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000	Size of user-programmable area, in bytes.

Table 10: Flash bank 0 information for the ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE

Notes:

1. Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.
2. Minimum value; may be larger if a different Flash memory device is fitted.
3. This value is guaranteed not to change.

Table 11 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	VPD space address [1]	Usage
0x0 - 0x7FFFFF	N/A	Alternate ADB3 PCI-E to OCP Bridge bitstream
0x800000 - 0xFFFFFF	N/A	Default ADB3 PCI-E to OCP Bridge bitstream
0x1000000 - 0x10FFFFF	0x0 - 0xFFFFF	Alpha Data VPD region [2, 4]
0x1100000 - 0x11FFFFF	0x100000 - 0x1FFFFF	Customer VPD region [3, 4]
0x1200000 - 0x28FFFFF	N/A	Target FPGA bitstream [5]
0x2900000 - 0x3FFFFFF	N/A	Failsafe target FPGA bitstream [6]

Table 11: Flash bank 0 address map for the ADM-XRC-6TL, ADM-XRC-6T1 & ADM-XRC-6TGE

Notes:

1. VPD space is the address space used by the API functions **ADMXRC3_ReadVPD** and **ADMXRC3_WriteVPD**.
2. Alpha Data programs this region with Vital Product Data (VPD) at manufacture-time.
3. Guaranteed not to be used for anything by Alpha Data. Any application-specific information can be stored here.
4. As a precaution against accidental writes, the Alpha Data supplied driver does not permit writes to this region unless a failsafe mechanism is disabled; refer to the release notes for the ADB3 driver for details.
5. Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND certain switches are set appropriately. Refer to the ADM-XRC-6TL / ADM-XRC-6T1 / ADM-XRC-6TGE user guide for details of the available switches.
6. Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up / reset, provided that this area is not blank AND one of the following conditions holds:
   (a) Configuration from the "Target FPGA bitstream" area is disabled via switches.
   (b) The "Target FPGA bitstream" area is blank.
   (c) The "Target FPGA bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

   In effect, this area stores a failsafe bitstream that is used if configuration with the "Target FPGA bitstream" cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. This is a precautionary measure against Negative Bias Temperature Instability (NBTI) effects.

10.2 ADM-XRC-6T-ADV8 Flash

The ADM-XRC-6T-ADV8 has a single bank of Flash memory with index 0 that is guaranteed to be at least 64 MiB in size. Alpha Data reserves the right to change the particular device used, but it is always a Common Flash Interface (CFI) device. An example of such a device is the Numonyx Axcell P30 Flash memory.

Table 12 shows the information returned by **ADMXRC3_GetFlashInfo(A|W)**:

Member	Possible values	Comment
Identifier [1]	"Numonyx Axcell P30 (Symm bl)"	String indicating what Flash memory device is fitted.
Size [2]	0x4000000	Size of Flash memory bank, in bytes.
UseableStart [3]	0x1200000	Byte offset within bank of start of user-programmable area.
UseableLength [2]	0x2E00000	Size of user-programmable area, in bytes.

Table 12: Flash bank 0 information for the ADM-XRC-6T-ADV8

Notes:

1. Not necessarily an exhaustive list; Alpha Data reserves the right to fit other Flash memory devices provided that the size is at least 64 MiB. This may be unavoidable if, for example, a particular device reaches end-of-life.
2. Minimum value; may be larger if a different Flash memory device is fitted.
3. This value is guaranteed not to change.

Table 13 below shows the address map, which is guaranteed not to change, for the Flash memory bank:

Flash byte address	Usage
0x0 - 0x1FFFFFF	Failsafe FPGA bitstream [2]
0x2000000 - 0x3FFFFFF	Default FPGA bitstream [1]

Table 13: Flash bank 0 address map for the ADM-XRC-6T-ADV8

Notes:

1. Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up.
2. Firmware will attempt to configure the target FPGA with a bitstream stored in this area at power-up, provided that one of the following conditions holds:
   (a) The "Default FPGA bitstream" area is blank.
   (b) The "Default FPGA bitstream" area is not blank, but configuration with the bitstream stored in that area failed.

   In effect, this area stores a failsafe bitstream that is used if configuration with the "Default FPGA bitstream" cannot be performed or fails. Alpha Data programs a valid bitstream at manufacture time so that the target FPGA cannot remain powered up and unconfigured for long periods. This is a precautionary measure against Negative Bias Temperature Instability (NBTI) effects.

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Revision History:

Date	Revision	Nature of Change
28/02/2011	1.0	Initial version
24/06/2011	1.1	Added information for ADM-XRC-6TGE. Corrected frequency range of ADM-XRC-6TL clock generator 0.
19/09/2011	1.2	Added information for ADM-XRC-6T-ADV8.

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