Using Xilinx Ultrascale MIG with the ADM-XRC-KU1

Document Revision: 1.2
29 Jun 2022

	Head Office	US Office
Address:	Suite L4A, 160 Dundee Street, Edinburgh, EH11 1DQ, UK	10822 West Toller Drive, Suite 250 Littleton, CO 80127
Telephone:	+44 131 558 2600	(303) 954 8768
Fax:	+44 131 558 2700	(866) 820 9956 - toll free
email:	sales@alpha-data.com	sales@alpha-data.com
website:	http://www.alpha-data.com	http://www.alpha-data.com

All trademarks are the property of their respective owners.

Table Of Contents

List of Tables

List of Figures

1 Introduction

This document describes how to customize and use the Xilinx DDR4 SDRAM Memory Interface Generator (MIG) IP (Vivado 2018.3.4 to 2022.1) in the ADM-XRC-KU1 reconfigurable computing card. Familiarity with the Vivado toolset is assumed. Code is generally presented as VHDL, but Verilog and SystemVerilog are equally valid as languages for developing an FPGA design and are compatible with the methodology presented in this document.

The ADM-XRC-KU1 is a reconfigurable computing card with a Kintex Ultrascale FPGA. Among other hardware features, it has four independent 32-bit wide banks of DDR4 SDRAM, each consisting of two 16-bit wide components.

Supported component types are given in Table 1 below.

Component	Component density	Speed	FPGA speed grade	Vivado version
MT40A512M16HA-083E	8 Gib (512 Mi x 16)	2400 MT/s (1200 MHz)	-2 or faster	2018.3 to 2022.1

Table 1 : Supported memory components
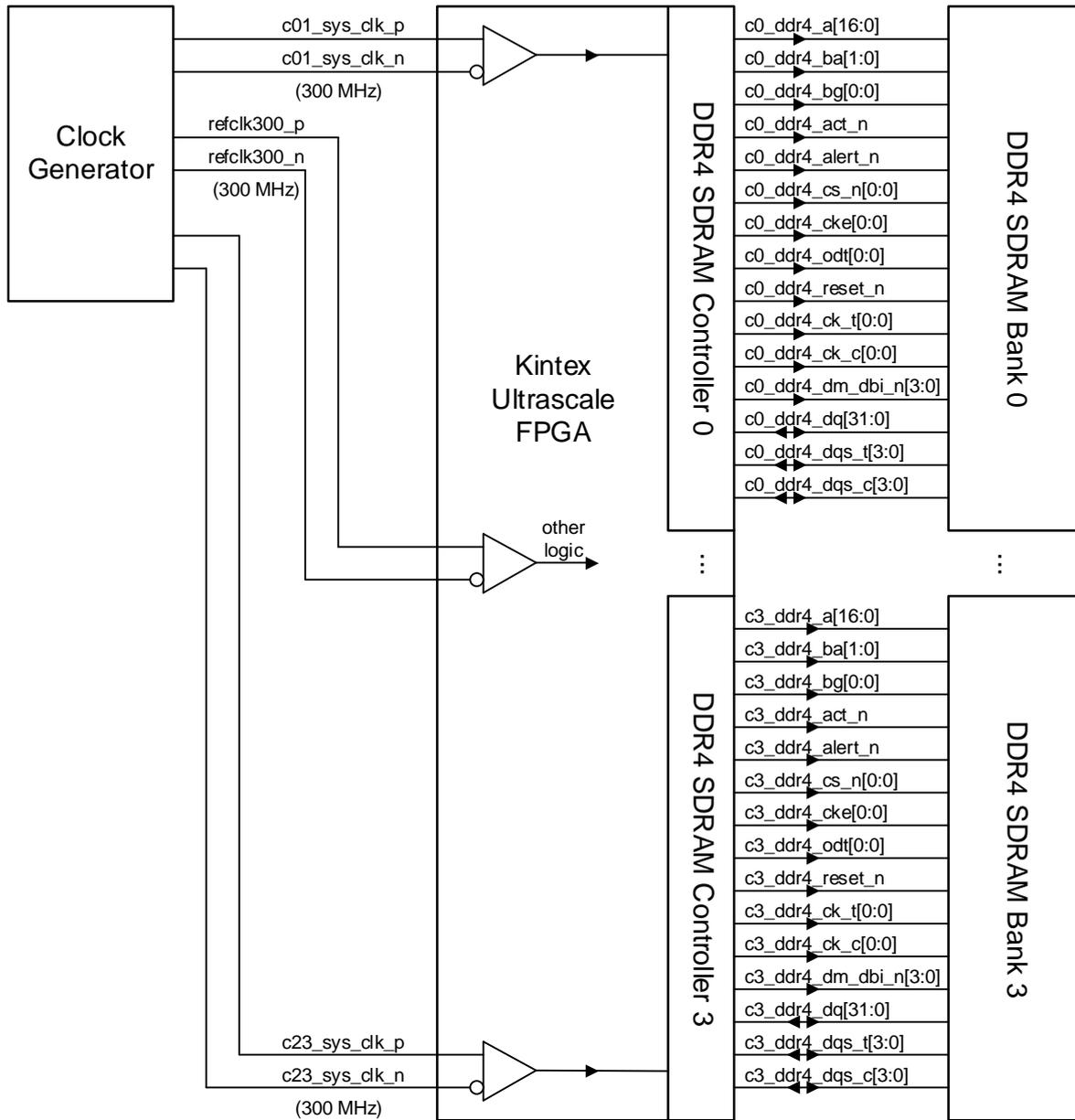
2 Memory architecture of the ADM-XRC-KU1

Figure 1 : Memory architecture of the ADM-XRC-KU1

The ADM-XRC-KU1 has eight DDR4 SDRAM components, arranged as four independent banks of memory.

The **canonical pinout**, consisting of all pins of a given bank of DDR4 SDRAM, is summarized by Table 2 below:

Port	Direction	Type
cN_ddr4_dq	inout	32-bit vector
cN_ddr4_dqs_t	inout	4-bit vector
cN_ddr4_dqs_c	inout	4-bit vector
cN_ddr4_a	out	17-bit vector

Table 2 : ADM-XRC-KU1 DDR4 SDRAM bank pinout (continued on next page)

Port	Direction	Type
cN_ddr4_ba	out	2-bit vector
cN_ddr4_bg	out	1-bit vector
cN_ddr4_act_n	out	bit
cN_ddr4_alert_n	in	bit
cN_ddr4_reset_n	out	bit
cN_ddr4_ck_t	out	1-bit vector
cN_ddr4_ck_c	out	1-bit vector
cN_ddr4_cke	out	1-bit vector
cN_ddr4_cs_n	out	1-bit vector
cN_ddr4_dm_dbi_n	out	4-bit vector
cN_ddr4_odt	out	1-bit vector
cN_ddr4_ten	out	bit
cN_ddr4_par	out	bit

Table 2 : ADM-XRC-KU1 DDR4 SDRAM bank pinout

In the above table, **N** is the bank number, 0, 1, 2 or 3.

For certain configurations of the DDR4 SDRAM (MIG) IP, the module generated by MIG has a **noncanonical pinout**, in which certain ports are omitted or have fewer bits, with respect to the canonical pinout. If a module generated by MIG has a noncanonical pinout, it is recommended to tie off any unused bits/ports of the canonical pinout to the appropriate logic levels (**0**, **1** or **Z**).

An example of a noncanonical pinout is the signals **cN_ddr4_ten**, **cN_ddr4_par** and **cN_ddr4_alert_n**; these ports are not present in the module generated by the Ultrascale DDR4 SDRAM (MIG) IP (as of Vivado 2015.4 to 2016.4).

IOSTANDARD, **SLEW** etc. constraints for the various pins are not given in the above table because they are automatically generated by MIG, and should not need to be changed.

2.1 ADM-XRC-KU1 300 MHz dedicated clock pins

The ADM-XRC-KU1 has a dedicated 300 MHz differential system clock for every two DDR4 SDRAM controllers. These clocks are buffered in user-created logic. Constraints for these clock pins must be in a user-created constraints file. Although it might be possible to use alternative system clock sources, Alpha Data recommends directly using the dedicated 300 MHz system clocks, because the quality of these clocks is a critical parameter in determining the reliability of the DDR4 SDRAM controllers.

Port	Direction	Type	Pin	IOSTANDARD
c01_sys_clk_p	in	bit	AK22	LVDS
c01_sys_clk_n	in	bit	AL22	LVDS
c23_sys_clk_p	in	bit	AN18	LVDS_25
c23_sys_clk_n	in	bit	AN17	LVDS_25

Table 3 : ADM-XRC-KU1 300 MHz dedicated clock pins

2.2 ADM-XRC-KU1 300 MHz reference clock pins

The ADM-XRC-KU1 has a 300 MHz reference clock which can be used for anything in the FPGA. In a typical FPGA design, it is buffered in user-created logic.

Port	Direction	Type	Pin	IOSTANDARD
refclk300_p	in	bit	AM21	LVDS
refclk300_n	in	bit	AN21	LVDS

Table 4 : ADM-XRC-KU1 300 MHz reference clock pins

3 Customizing Ultrascale DDR4 SDRAM (MIG) IP for the ADM-XRC-KU1 from scratch

This section illustrates creating a customized Ultrascale DDR4 SDRAM (MIG) IP **.xci** file for the ADM-XRC-KU1 from scratch.

Please refer to the following subsection that is appropriate to the version of the Vivado tools that you are using.

3.1 Vivado 2018.3 or later

The sequence of screen captures below walks the user through the tabs of the Ultrascale DDR4 SDRAM (MIG) customization GUI. Options that are of interest or must be changed to an appropriate value are highlighted by colored or black boxes, according to the following scheme:

- A black box draws attention to something, which may be a read-only value.

- A yellow box highlights an option that must be set exactly one way, as shown in the screen capture.

- A blue box highlights an option that can be set in various ways, and is discussed in the accompanying text.

3.1.1 Ultrascale DDR4 SDRAM (MIG) IP customization - Basic options (2018.3)

Figure 2 : Ultrascale DDR4 SDRAM (MIG) IP customization - Basic options (2018.3)

The **Data Mask and DBI** option determines whether or not the data byte inversion (DBI) feature is used. It is recommended to set this to either **DM NO DBI** or **DM DBI RD**, because this permits masked writes to be performed.

The **Memory Address Map** and **Ordering** options are at the discretion of the user.

The options **Force Read and Write commands ...**, **Enable AutoPrecharge Input** and **Enable User Refresh and ZQCS Input** are normally left unchecked. In certain usage scenarios there may be a performance advantage to checking some of them, but this is an advanced topic that is outside the scope of this document.

The **AXI4 Interface** option can be checked or unchecked as appropriate. If checked, additional options are

presented, as shown in Figure 3. It is recommended that **Data Width** is set to **256** to maximise the AXI4 throughput to the DDR4 SDRAM controller.

Figure 3 : Ultrascale DDR4 SDRAM (MIG) IP customization - AXI4 options (2018.3)

3.1.2 Ultrascale DDR4 SDRAM (MIG) IP customization - Advanced options (2018.3)

Figure 4 : Ultrascale DDR4 SDRAM (MIG) IP customization - Advanced options (2018.3)

With the exception of **Reference Input Clock Configuration**, which must be set as in Figure 4, the options are at the discretion of the user.

4 Known issues

4.1 MIG DDR4 SDRAM controllers with shared system clock cannot be reset independently

In the ADM-XRC-KU1, the MIG DDR4 SDRAM controllers for banks 0 and 1 share a 300 MHz system clock, from which they derive several clocks used internally. Similarly, the MIG DDR4 SDRAM controllers for banks 2 and 3 share another 300 MHz system clock. In Vivado 2018.3 to 2022.1, bank 0 or bank 1 cannot be reset independently without causing the other bank in the pair to malfunction. Similarly, bank 2 or bank 3 cannot be reset independently without causing the other bank in the pair to malfunction.

Because this issue is unlikely to be problematic for a typical FPGA design, which is expected to use a common reset signal for all four DDR4 SDRAM controllers, no workaround is presented here. It is recommended that (at least) each pair of banks share a common reset signal.

This issue may be resolved in a future version of Vivado / Ultrascale MIG DDR4 SDRAM Controller IP.

Revision History

Date	Revision	Nature of change
22 June 2016	1.0	Initial version.
17 Jan 2017	1.1	Updated for Vivado 2016.4.
29 Jun 2022	1.2	Updated for Vivado 2018.3 to 2022.1.