ADM-XRC-KU1 Support & Development Kit

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1 Introduction

The **ADM-XRC-KU1 Support & Development Kit (SDK)** is a set of resources for FPGA designers and software engineers working with Alpha Data's ADM-XRC-KU1 reconfigurable computing card.

The resources of the ADM-XRC-KU1 SDK include:

- Resources for developing application software for a machine that hosts Alpha Data reconfigurable computing hardware:
  - C/C++ header files and libraries which provide Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Documentation about Application Programming Interfaces (APIs) for controlling reconfigurable computing hardware.
  - Common utilities (with source code) for viewing information about reconfigurable computing devices, programming nonvolatile memory, and more.
- Example FPGA designs and host programs (with source code) demonstrating various features of the ADM-XRC-KU1:
  - The **Standalone DDR4 Test FPGA Design** demonstrates how to use the onboard DDR4 SDRAM memories.
  - The **DMA Demonstration FPGA Design** demonstrates how to use the DMA channels (AXI4) of Alpha Data's **ADM-XRC-KU1-HSAXI** IP in order to transfer between the target FPGA and the host, via the PCIe to MPTL Bridge.
  - The **DMA Demonstration (PCIe) FPGA Design** demonstrates the use of Alpha Data's **ADM-XRC-KU1-P5HI** IP, which includes a PCI Express endpoint with DMA engines (AXI4) for the XMC P5 connector.
  - The **Interrupt Test FPGA Design** demonstrates the FPGA interrupt mechanism, whereby an event within user-defined logic in the target FPGA can result in delivery of a notification to host software.
  - The **Simple Demonstration FPGA Design** contains a more or less minimal set of logic, including **ADM-XRC-KU1-HSAXI**, that enables the host CPU to read and write register in the target FPGA, via the PCIe to MPTL Bridge.
  - The **Simple Demonstration (OCP) FPGA Design** is functionally similar to **Simple Demonstration FPGA Design**, but uses OCP protocol and the **ADM-XRC-KU1-HSOCP** IP. It is provided in order to ease migration from Alpha Data's earlier reconfigurable computing products.
- IP and common HDL code for the target FPGA, provided by Alpha Data:
  - **ADM-XRC-KU1-HSAXI** Host Interface IP, which provides an MPTL to AXI4 interface with DMA channels, as well as other features. This allows the host CPU to exchange data with the target FPGA via the PCIe to MPTL Bridge.
  - **ADM-XRC-KU1-HSOCP** Host Interface IP, which provides an MPTL to OCP interface with DMA channels, as well as other features. This IP performs a similar function to **ADM-XRC-KU1-HSAXI**, but with OCP protocol rather than AXI4, and is provided in order to ease migration from Alpha Data's earlier reconfigurable computing products.
  - **ADM-XRC-KU1-P5HI** PCIe Host Interface IP, which provides a PCI Express to AXI4 interface with a configurable number of DMA engines (AXI4), as well as other features, in the target FPGA. This is provided for applications which transfer data to the target FPGA via the XMC P5 connector whilst bypassing the PCIe to MPTL Bridge.
  - **ADM-XRC-KU1-P6HI** PCIe Host Interface IP, which provides a PCI Express to AXI4 interface with a configurable number of DMA engines (AXI4), as well as other features, in the target FPGA. This is provided for applications which transfer data to the target FPGA via the XMC P6 connector whilst bypassing the PCIe to MPTL Bridge.
  - Common HDL code (i.e. not specific to the ADM-XRC-KU1), used by the example FPGA designs.

1.1 Structure of this package

The directories making up the ADM-XRC-KU1 SDK are organised as in Figure 1 below:

- **(root)** .... *The root of this SDK*
  - **doc/** .... *Contains this document*
  - **example/**
    - **ddr4_test-admxrcku1-v1_1_0/** .... *Standalone DDR4 Test FPGA Design*
    - **dma_demo-admxrcku1-v1_2_0/** .... *DMA Demonstration FPGA Design*
    - **dma_demo_pcie-admxrcku1-v1_2_0/** .... *DMA Demonstration (PCIe) FPGA Design*
    - **itest-admxrcku1-v1_1_0/** .... *Interrupt Test FPGA Design*
    - **simple-admxrcku1-v1_2_0/** .... *Simple Demonstration FPGA Design*
    - **simple_ocp-admxrcku1-v1_2_0/** .... *Simple Demonstration (OCP) FPGA Design*
  - **fpga/**
    - **lib/** .... *Common HDL code*
    - **repo/** .... *Repositories for Vivado IP*
  - **host/**
    - **api-v1_4_21/** .... *Header files and libraries for APIs*
    - **app_framework-v1_4_0/** .... *Framework used by host programs of example FPGA designs*
    - **util-v1_13_0/** .... *Common Host Utilities*

Figure 1 : Structure of the SDK

2 Recommended Vivado versions

For this release of the ADM-XRC-KU1 SDK, recommended Vivado versions for the example FPGA designs are as follows:

Example FPGA design	Short name	Compatible tool versions	Recommended tool version
Standalone DDR4 Test FPGA Design	ddr4_test	2018.3 or later	2022.1
DMA Demonstration FPGA Design	dma_demo	2018.3 or later	2022.1
DMA Demonstration (PCIe) FPGA Design	dma_demo_pcie	2018.3 or later	2022.1
Interrupt Test FPGA Design	itest	2018.3 or later	2022.1
Simple Demonstration FPGA Design	simple	2018.3 or later	2022.1
Simple Demonstration (OCP) FPGA Design	simple_ocp	2018.3 or later	2022.1

In this release of the SDK, Vivado 2022.1 was used to generate pre-built bitstreams.

3 Development operating system support

3.1 Windows

Generally speaking, Alpha Data's Windows software, when supplied in binary form, is compatible with Windows XP and later. However, the choice of Windows operating system used for development mainly depends upon which releases of Microsoft Visual Studio and/or Xilinx Vivado are chosen for a project.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore a Windows operating system must be capable of running Vivado. As of writing, Vivado 2022.1 is the current release and supported Windows operating systems are given in the the Vivado 2022.1 release notes:

https://www.xilinx.com/support/documentation/sw_manuals/xilinx2022_1/ug973-vivado-release-notes-install-license.pdf

Vivado path length issue

In Windows, Vivado requires that path lengths of files are no greater than the **MAX_PATH** Win32 constant, which is 260 characters (including the NUL character used to terminate a string). This limit is easily exceeded when a Vivado project uses IP (cores) and the path length of the Vivado project file (.xpr) exceeds about 80 characters. Exceeding the **MAX_PATH** limit can result in otherwise inexplicable failures when implementing an FPGA design in Vivado.

The recommended workaround for this issue is to use the **subst** command to map a drive letter (e.g. **Z:**) to the root of this SDK. If done correctly, the result is the existence of directories **Z:\doc**, **Z:\example**, **Z:\fpga** etc.

When developing software to run on a host machine, Microsoft Visual Studio is likely to be used for building applications. Therefore, the Windows operating system must be capable of running a particular version of Microsoft Visual Studio. For Microsoft Visual Studio 2012 or 2013, Windows 7, Windows 8.1 and Windows 10 are recommended.

3.2 Linux

Alpha Data generally does not supply binaries for Linux because of the large number of architectures and configurations that exist across various Linux distributions. Source code is provided, however, and can be built for most Linux distributions.

When developing an FPGA design, the Xilinx Vivado toolset is used and therefore the supported Linux distributions depend upon the release of Vivado chosen for a project. As of writing, Vivado 2022.1 is the current release and supported Linux distributions are given in the Vivado 2022.1 release notes:

https://www.xilinx.com/support/documentation/sw_manuals/xilinx2022_1/ug973-vivado-release-notes-install-license.pdf

4 Conventions used in this SDK

4.1 Version numbers

If the name of a folder in the SDK has a suffix such as **v1_0_0**, it denotes a version number for that subtree as a whole.

4.2 Common HDL code

The folder **fpga/lib/** contains common HDL code used by certain example FPGA designs. Within this folder, each component (a collection of HDL source files) is a subtree whose name has a version suffix (for example, **fifo-v1_0_0/**.

4.3 Vivado IP repositories

The folder **fpga/repo/** contains Vivado IP repositories used by certain example FPGA designs. Generally speaking, if this folder contains a subfolder **vivado-*XXXX.Y*/**, it means that the IP-XACT definitions found within it are compatible with Vivado *XXXX.Y* or later.

The folder **fpga/repo/interfaces/** might exist in some SDKs. This folder contains IP-XACT interface definitions, which are generally compatible with any version of Vivado.

4.4 Example FPGA designs

The example FPGA designs, found in the **example/** folder, consist of the following elements:

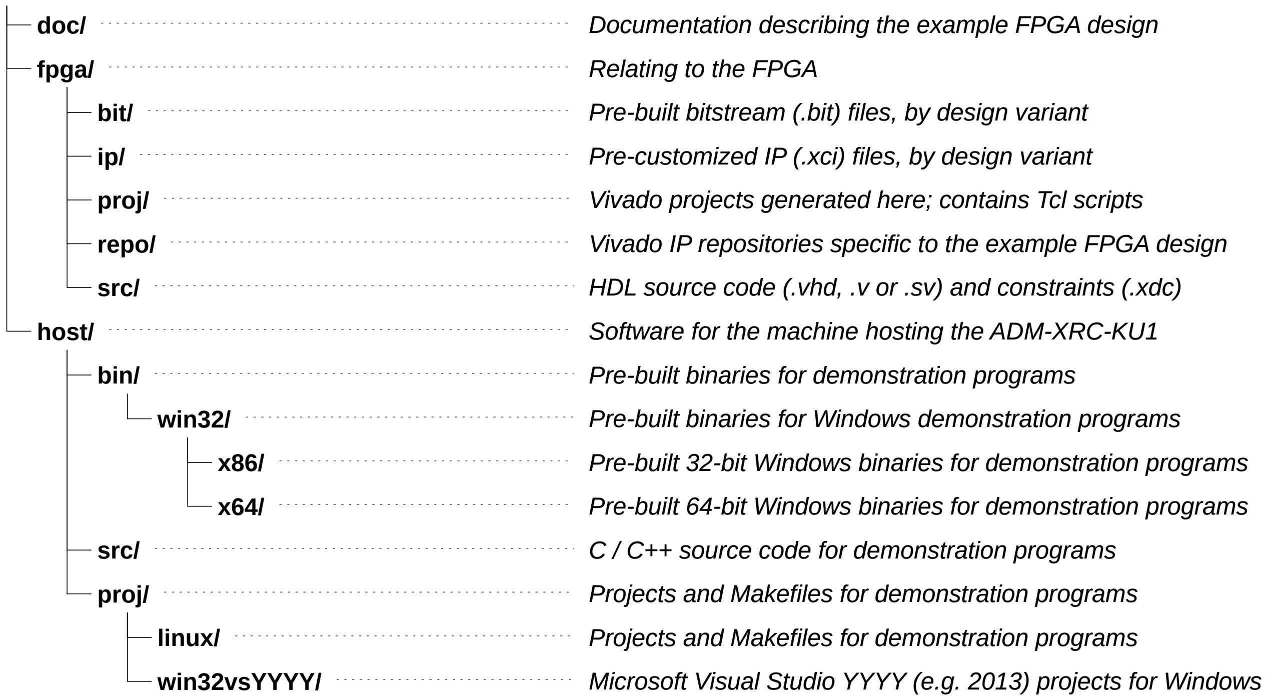
- Documentation describing the example FPGA design.
- FPGA-related:
    - HDL source code (VHDL / Verilog / SystemVerilog).
    - Constraints (.xdc files).
    - Tcl scripts for generating Vivado projects; ready-made Vivado projects are not supplied.
    - Pre-built bitstream files (**.bit**), generally built with the latest version of Vitis / Vivado available at time of publication.
- Host-related, if appropriate for the example FPGA design in question:
    - C / C++ source and header files.
    - Project files for Microsoft Visual Studio and Makefiles for Linux, where supported for the example FPGA design in question.
    - Pre-built binaries, for Windows running on Intel architecture, if supported for the example FPGA design in question.
    - For Linux, there are so many possible architectures, binary formats, compilers, environmental issues and other build options that supplying binaries is deemed impractical. For these operating systems, the user must compile demonstration programs before running them.

As mentioned above, ready-made Vivado projects are not supplied in this SDK. Tcl scripts for generating Vivado projects are provided instead for the following reasons:

- Tcl scripts are more compact and portable than Vivado projects; a Vivado project generated in Windows might not work correctly in Linux, and vice versa.
- Tcl scripts can automate the application of workarounds for issues specific to particular Vivado versions.

The structure of each example FPGA design conforms to the following general template:

<design>-<board>-<version> .... *The root of the example FPGA design*



doc/	*Documentation describing the example FPGA design*
fpga/	*Relating to the FPGA*
bit/	*Pre-built bitstream (.bit) files, by design variant*
ip/	*Pre-customized IP (.xci) files, by design variant*
proj/	*Vivado projects generated here; contains Tcl scripts*
repo/	*Vivado IP repositories specific to the example FPGA design*
src/	*HDL source code (.vhd, .v or .sv) and constraints (.xdc)*
host/	*Software for the machine hosting the ADM-XRC-KU1*
bin/	*Pre-built binaries for demonstration programs*
win32/	*Pre-built binaries for Windows demonstration programs*
x86/	*Pre-built 32-bit Windows binaries for demonstration programs*
x64/	*Pre-built 64-bit Windows binaries for demonstration programs*
src/	*C / C++ source code for demonstration programs*
proj/	*Projects and Makefiles for demonstration programs*
linux/	*Projects and Makefiles for demonstration programs*
win32vsYYYY/	*Microsoft Visual Studio YYYY (e.g. 2013) projects for Windows*

Figure 2 : Structure of the SDK

Certain example designs might omit certain folders or include additional folders; for example, the **ddr4_test** FPGA Design omits the **host/** folder because it has no host interface and is driven solely by Vivado Hardware Manager.

4.4.1 Vivado Tcl script naming conventions

Within the **fpga/proj/** folder of each example FPGA design, a number of Tcl scripts are provided. Most important are the Vivado project-generation scripts, whose filenames begin with the prefix **mkxpr** and include a suffix that identifies a particular *design variant*. The commonly-provided Tcl scripts are given in Table 1 below.

General form of filename of Tcl script	Purpose
build-*<design variant>*.tcl	Implements the design in Vivado for a particular design variant
debug-*<design variant>*.tcl	Opens Vivado Hardware Manager and boots the FPGA in a card with the **.bit** file for a particular design variant. These scripts can usually also be found in the **fpga/bit/*<design variant>*** folders of a given example FPGA design.
mkxpr-*<design variant>*.tcl	Generates a Vivado project for a particular design variant.
rebuild-*<design variant>*.tcl	Re-implements the design in Vivado for a particular design variant

Table 1 : Commonly-provided Vivado Tcl scripts

Design variants allow for several variations to exist for a given example FPGA design. For example, a given example FPGA design might include (i) "normal" variants which omit debug / instrumentation logic and (ii) instrumented variants which include debug / instrumentation logic.

In general, the total number of design variants for a given example FPGA design is the result of enumerating the valid combinations of one or more "orthogonal" options.

5 Associated documents

(1) Common Host Utilities for Windows & Linux
(root)/host/util-v1_13_0/doc/ad-ug-0055_v1_4.pdf

(2) Common Host Utilities for VxWorks
(root)/host/util-v1_13_0/doc/ad-ug-0086_v1_2.pdf

(3) ADMXRC3 API Specification
(root)/host/api-v1_4_21/doc/ad-ug-0003_v1_13.pdf

(4) ADMXRC3 API Hardware Addendum
(root)/host/api-v1_4_21/doc/ad-ug-0009_v1_12.pdf

(5) ADM-XRC-KU1 Standalone DDR4 Test FPGA Design
(root)/example/ddr4_test-admxrcku1-v1_1_0/doc/ad-ug-0058_v1_3.pdf

(6) Using Xilinx Ultrascale MIG with the ADM-XRC-KU1
(root)/example/ddr4_test-admxrcku1-v1_1_0/doc/ad-ug-0059_v1_2.pdf

(7) ADM-XRC-KU1 DMA Demonstration FPGA Design
(root)/example/dma_demo-admxrcku1-v1_2_0/doc/ad-ug-0067_v1_3.pdf

(8) ADM-XRC-KU1 DMA Demonstration (PCIe) FPGA Design
(root)/example/dma_demo_pcie-admxrcku1-v1_2_0/doc/ad-ug-0069_v1_3.pdf

(9) ADM-XRC-KU1 Interrupt Test FPGA Design
(root)/example/itest-admxrcku1-v1_1_0/doc/ad-ug-0104_v1_1.pdf

(10) ADM-XRC-KU1 Simple Demonstration FPGA Design
(root)/example/simple-admxrcku1-v1_2_0/doc/ad-ug-0060_v1_3.pdf

(11) ADM-XRC-KU1 Simple Demonstration (OCP) FPGA Design
(root)/example/simple_ocp-admxrcku1-v1_2_0/doc/ad-ug-0079_v1_3.pdf

6 Release history

6.1 Release 1.1.0

Enhancements:

1. Refreshed example FPGA designs so that they can be generated and built with Vivado 2018.3 to 2022.1.
2. The Interrupt Test FPGA Design (itest) example is now included in this SDK, instead of being a separately downloaded example.
3. Certain Alpha Data IPs have been updated:
    - (a) ADM-XRC-KU1-P5HI (PCIe endpoint core for XMC P5 connector) has been updated from version 1.0 to 1.1.
    - (b) ADM-XRC-KU1-P6HI (PCIe endpoint core for XMC P6 connector) has been updated from version 1.0 to 1.1.
    - (c) ADM-XRC-KU1-HSAXI (MPTL interface core with AXI interfaces) has been updated from version 1.1 to 1.4.3.
    - (d) ADM-XRC-KU1-HSOCP (MPTL interface core with OCP interfaces) has been updated from version 1.1 to 1.4.3.

6.2 Release 1.0.0

Enhancements:

1. The API header files and libraries for host programs has been updated to version 1.4.18b4. This adds the <avr2.h> API header file, which is used by **AVR2UTIL** common host utility to implement USB communications with the microcontroller.
2. The Common Host Utilities can now be built for VxWorks, and their collective version number is now 1.10.0.
3. In Windows & Linux but not VxWorks, the **AVR2UTIL** common host utility can now communicate with the microcontroller on supported models via a USB connection as well as via PCIe. The set of commands that it provides has also been expanded.
4. The host program for each of the example designs **dma_demo-admxrcku1**, **dma_demo_pcie-admxrcku1**, **simple-admxrcku1** & **simple_ocp-admxrcku1** has been updated to use the latest API header files and libraries (1.4.18b4). These example designs are now at version 1.1.0.

6.3 Release 0.1.0

This is the first release of the ADM-XRC-KU1 Support & Development Kit.

Revision History

Date	Revision	Nature of change
21 Jul 2016	1.0	Initial version.
30 Aug 2016	1.1	Updated for 1.0.0 release: Common Host Utilities for VxWorks now included.
09 Aug 2022	1.2	Updated for 1.1.0 release: Refreshed example designs for Vivado 2022.1.