Alpha Data Blockset for System Generator

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1 Introduction

This document decribes the reference design provided in the Alpha Data Blockset for System Generator v4.1. This is not strictly a blockset as no Simulink blocks are provided. The reference design instead provides an example ISE project with an System Generator DSP core. All the complex multi-clock domain, external hardware interfacing IP is kept in the VHDL wrapper. This means that the System Generator DSP core requires only a single clock domain and interfaces with high performance off chip hardware through data streaming interfaces, simplifying development, allowing the System Generator user to focus on the DSP problems at hand thus improving rapid prototyping. In this release, example code is provided for the ADM-XRC-6T1, ADPE-XRC-6T and ADPE-XRC-6TL boards only.

The example code is dependent on modules from ADMXRCG3-SDK. The latest version should be used, however the archived projects contain a working snapshot of the required files referenced as remote sources.

2 Getting Started

The top level of the project should be opened in ISE Project Navigator (not System Generator). Archived projects can be found in the boards folder with a different project available for each target board. The following instructions apply specifically to the ADM-XRC-6T1 project, however there are only a few differences with the other boards due to the smaller number of memory banks fitted.

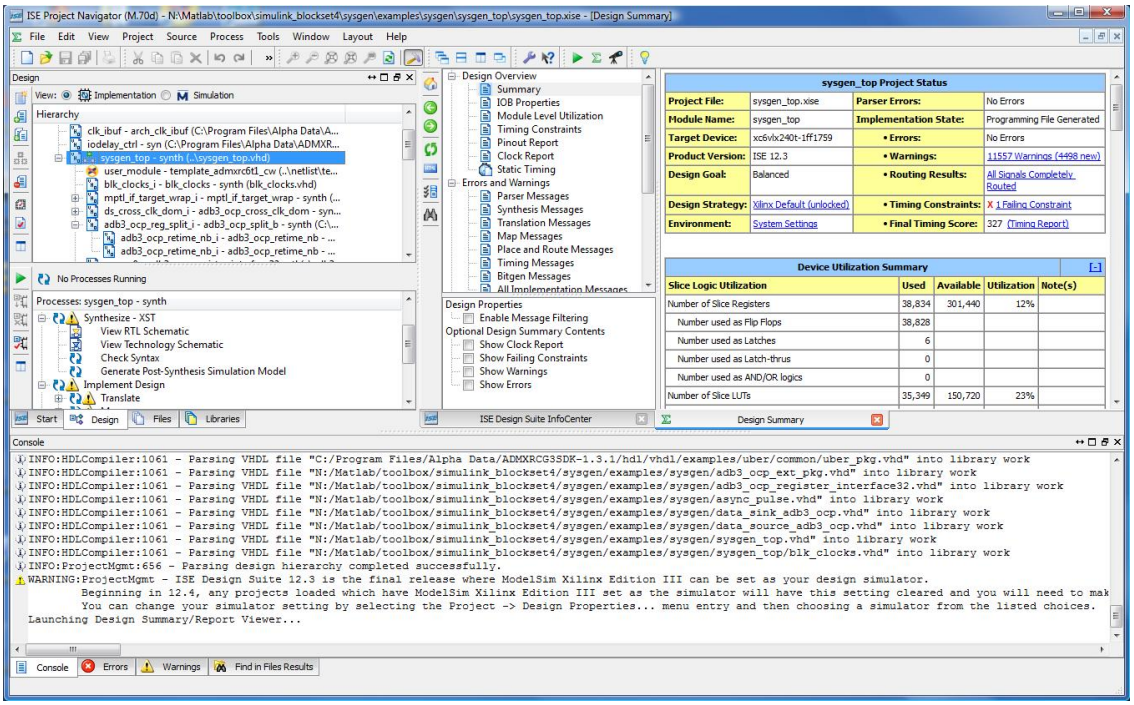

Figure 1: Sysgen Top ISE Project

Figure 1 shows the ISE project when opened in ISE Project Navigator. Clicking on the sysgen_top module makes available all the Synthesis option available allowing the design to be built into a bitstream.Note the user_module, with a SysGen Icon. This is the System Generator part of the design which can be edited using System Generator. Click on this to reveal the options available for this block as shown in Figure 2.

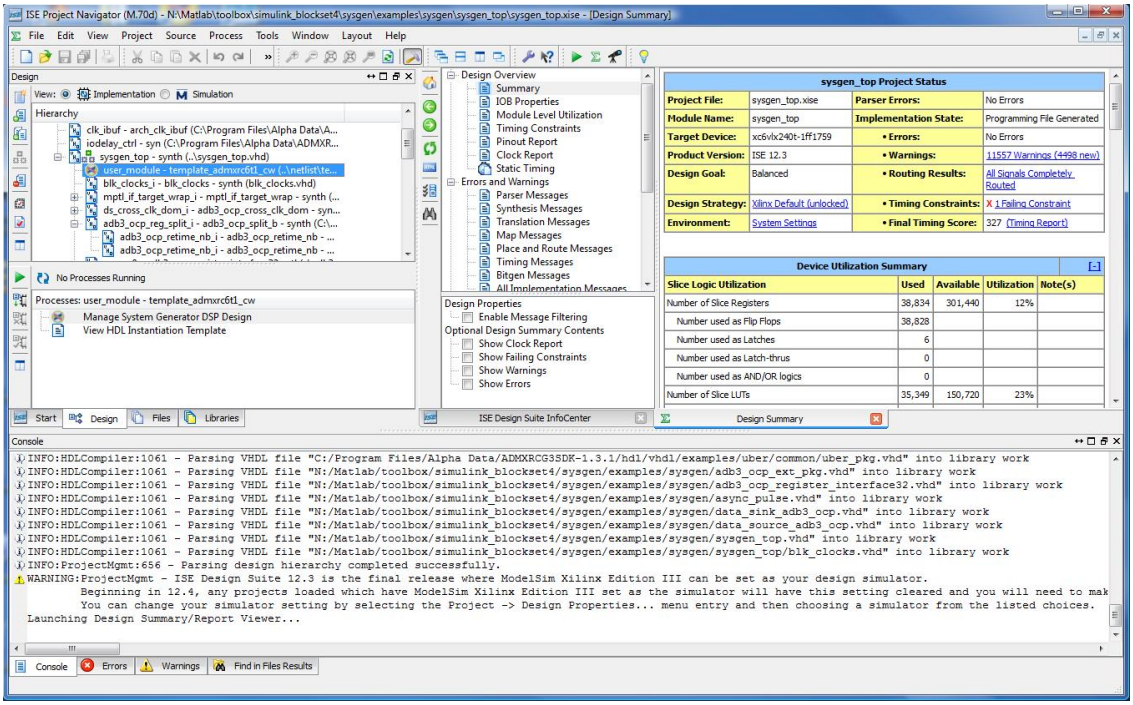

Figure 2: Sysgen ISE Options

When the Sysgen user_module block is selected, the option to "Manage System Generator Design" becomes available. Selecting this runs Matlab and Simulink and opens the Sysgen project.

3 The SysGen User Module

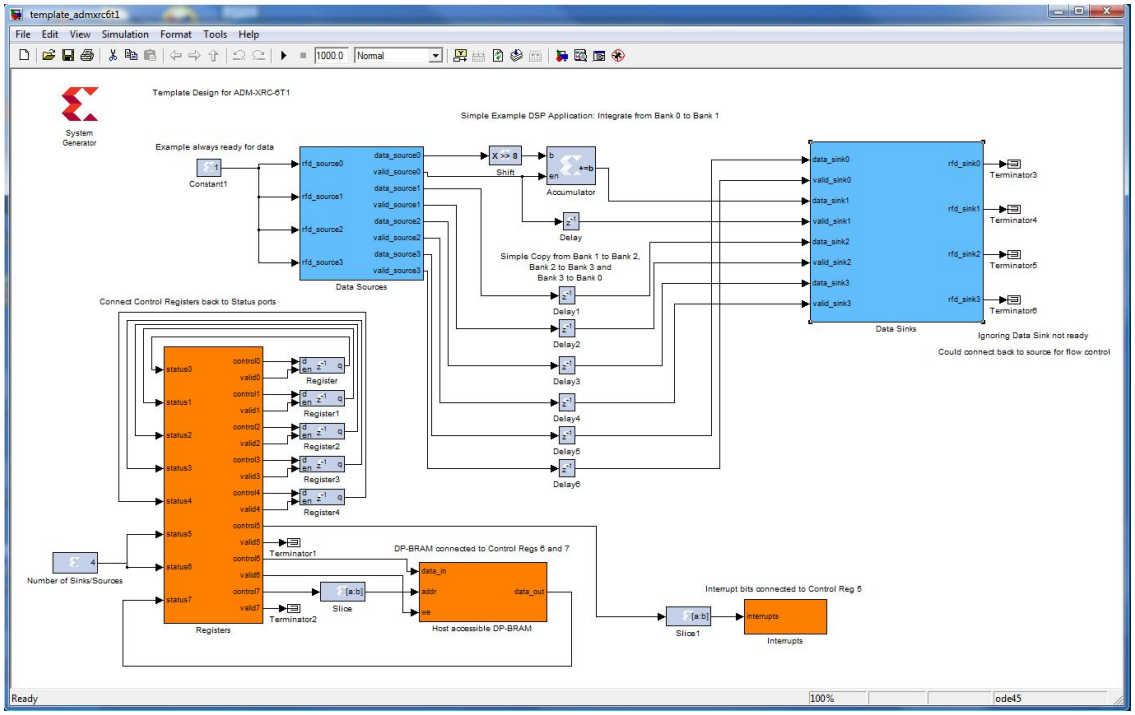

Figure 3: Sysgen ISE Options

The example Sysgen project "template_admxrc6t1" is shown in figure 3. This design contains a number of blocks which define the interface between the System Generator module and the wrapper modules whihc handle the IO.

3.1 Registers

This block contains a number of input and output ports connected to 8 host accessible registers. These are designed to allow small amounts of configuration and status data to be passed between the host and the user FPGA application.

For example, the registers could be used in a DDC (Digital Down Converter) to set frequency paramaters or the band of interest

3.2 Host accessible DP-BRAM

This block contains a 512x32bit memory block which can be accessed both by the host and by the Sysgen FPGA user application. This block is for data transfers too large for the regiter block.

For example, the DP-BRAM could be used to initialise filter co-efficients for a re-programmable filter

3.3 Interrupts

This block outputs 24 level sensitive interrupts to the top level. The top level has a mask register for these 24 interrupts, along with 8 from the Data Sink and Sources. These allow the FPGA to interrupt the host and notify it of an event without requiring the host to continuously poll a status register.

3.4 Data Sources

The data sink and data source blocks provide an interface to the on-board SDRAM, through a simple stream based interface. This is ideal for most DSP applications where filtering of a stream of samples is required.

The data sources block contains 4 data source ports, which will provide data with a valid strobe. A rfd (ready for data) strobe is provided to POP data from the source interface and provide flow control if required.

The data source block in hardware works by reading successive addresses in SDRAM, and pushing the data into a asynchronous FIFO 32 bits wide, the output of which is available to the User application. The start and stop addresses to read, whether the source runs continually, and whether an interrupt is generated at the end of data (or midway through) is controlled via host software. The interrupts can be used to trigger a DMA upload of the next section of data to allow continuous stream processing.

3.5 Data Sinks

The data sinks block provides 4 data sink ports. Each of these is set up to act as a data capture engine, recording signals (when the valid is asserted) and storing them in SDRAM memory. The rfd_flag may be asserted if the data rate exceeds what can be stored in SDRAM, and so should be monitored in high bandwidth situations. Note that the Data Sink rate is by default 4 bytes at 160MHz, whereas the SDRAM access is 16 bytes wide at 200MHz, although this is shared with the source module and any host access as well.

While data sinks and sources do not provide fully flexible memory access to the SDRAM, they do make the implementation of typical signal processing apllications (such as recording an A2D input signal with some basic signal processing) much easier to implement.

3.6 Simulation Code

The above mentioned interface block contain some fairly trivial simulation code. The purpose of this code is not to simulate the operation of the outer parts of the FPGA design, but to generate test signals appropriate to the DSP design built with the template. Therefore rather than simulating the host writing a sine wave to SDRAM memory, followed by the FPGA reading the sine wave, the simulation only generates the sine wave data at the interface to the System Generator module.

3.7 Compilation

Double clicking on the System Generator Token brings up the Compilation options allowing the System Generator Template design to be compiled into a VHDL sub-module of the whole design. Comilation should be HDL Netlist, with XST as the Synthesis tool and VHDL as the Hardware Description Language. The target directory should be ./netlist.

3.8 Modifying I/O

In many cases users will want to modify the I/O to allow, for example, the addition of an external A2D input. In the system generator side this should simply be a case of adding an input gateway. The Pin location constraints should however be added at the top level UCF and not in the Sysgen port. The sysgen_top.vhd design will also have to be modified to match. In cases where the pins can be directly connected, this will just mean adding the signals to the sysgen_top.vhd design and the user_module block. This approach also allows more complex I/O HDL to be added between the Sysgen design and the pins to support external devices which require tri-state, DDR or asynchronous clock domain crossing connections at the pins, whcih cannot be handled internally by SysGen code.

4 Wrapper Code

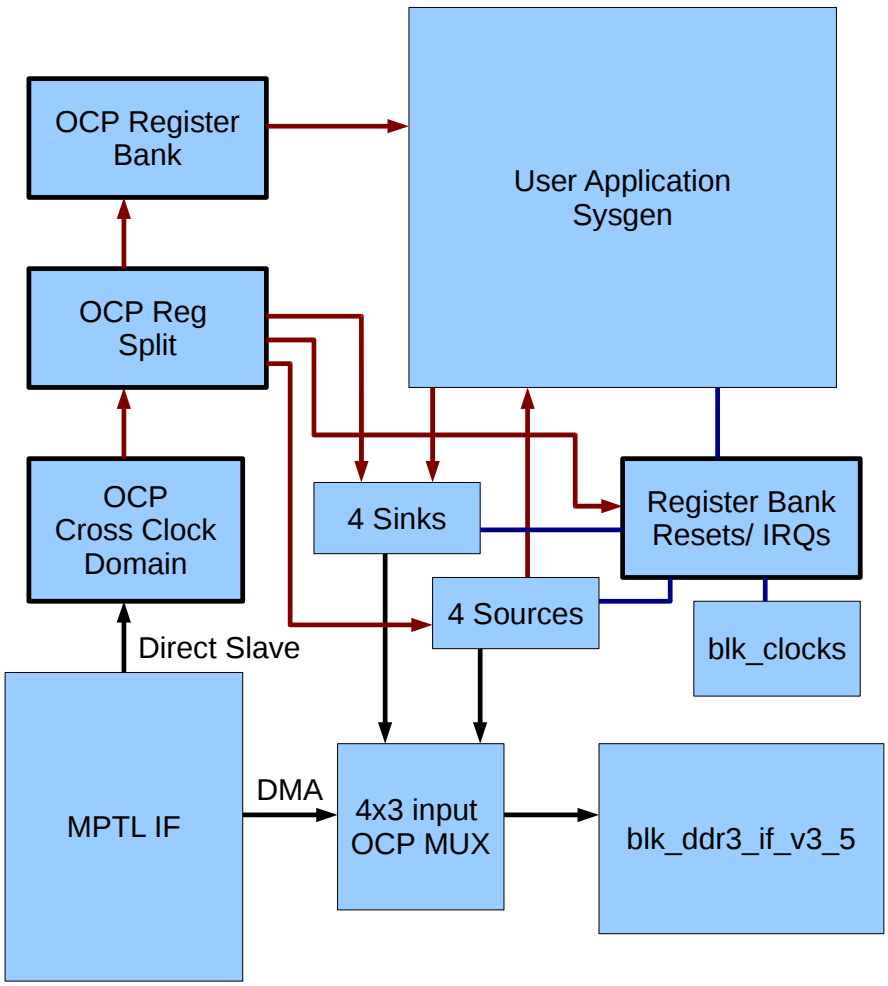

Figure 4: Sysgen Reference Design Block Diagram

The wrapper code is contained in top level VHDL file sysgen_top.vhd. A block diagram for this file is shown in Figure 4.

This shows the connections between the PCIe Host IF (MPTL IF), and the registers via the Direct Slave port, which is mapped as a 4MB widow in PCIe space. The connections between the host and the SDRAM blocks is only through the DMA channels, and is best suited for large fast transfers of data. The Memory access for each o the 4 banks is split between 1 DMA channel, 1 data source and 1 data sink.

In general the only VHDL modules users should find themselves modifying are the sysgen_top.vhd to add external I/O ports or to change sink/source data widths or the blk_clocks module, which can be modififed to change the pll_reg_clk frequnecy, used by the system generator design. This can be easily performed by modifying the PLL parameters. If this is cahnged the clock period specification in the .xcf file must also be modified.

The default UCF file is for the lx240t device. This file will also support the lx365t and sx315t devices. Users with lx550t or sx475t devices should change the UCF file to sysgen_top-admxrc6t1-6vlx550t.ucf as the SDRAM controller location constarints are slightly different for these devices.

5 Host Software

In the software directory, a simple MSVC project is included with a basic test application which tests the functionality of the reference design. This application does some basic read and write tests for the Sysgen user registers and the shared BRAM. It also performs bank to bank memory tests, using the sinks and sources. The code also uploads and downloads data from the host to the SDRAM banks. The program also performs an interrupt test to verify the operation of the sysgen user interrupts.

The main program is in test_template.c which should be used with the header file test_template.h. This header file is useful as it has definitions for the template designs memory map, which is shown in the register map below

5.1 ADM-XRC-6T1 Reference Design for System Generator

Register	Offset	Description
SYSGEN_REG0	0x0000	User defined Sysgen Block Register
SYSGEN_REG1	0x0004	User defined Sysgen Block Register
SYSGEN_REG2	0x0008	User defined Sysgen Block Register
SYSGEN_REG3	0x000C	User defined Sysgen Block Register
SYSGEN_REG4	0x0010	User defined Sysgen Block Register
SYSGEN_REG5	0x0014	User defined Sysgen Block Register
SYSGEN_REG6	0x0018	User defined Sysgen Block Register
SYSGEN_REG7	0x001C	User defined Sysgen Block Register
IRQ_STATUS	0x0100	Interrupt Status Register, Write to Clear
IRQ_ENABLE	0x0104	Interrupt Enable Register
SINKS_FLUSH_PACKET	0x0108	Sink flush strobes
SINK0_START_ADDR	0x2000	Start address for storing data captured in sink 0
SINK0_WORD_LIMIT	0x2004	Limit of 16 byte words of data to be captured by sink 0
SINK0_IRQ_LIMIT	0x2008	Number of 32 bit words of data received before generating IRQ from sink 0
SINK0_CONTROL	0x200C	Control register for sink 0
SINK1_START_ADDR	0x2100	Start address for storing data captured in sink 1
SINK1_WORD_LIMIT	0x2104	Limit of 16 byte words of data to be captured by sink 1
SINK1_IRQ_LIMIT	0x2108	Number of 32 bit words of data received before generating IRQ from sink 1
SINK1_CONTROL	0x210C	Control register for sink 1
SINK2_START_ADDR	0x2200	Start address for storing data captured in sink 2
SINK2_WORD_LIMIT	0x2204	Limit of 16 byte words of data to be captured by sink 2
SINK2_IRQ_LIMIT	0x2208	Number of 32 bit words of data received before generating IRQ from sink 2
SINK2_CONTROL	0x220C	Control register for sink 2
SINK3_START_ADDR	0x2300	Start address for storing data captured in sink 3
SINK3_WORD_LIMIT	0x2304	Limit of 16 byte words of data to be captured by sink 3
SINK3_IRQ_LIMIT	0x2308	Number of 32 bit words of data received before generating IRQ from sink 3
SINK3_CONTROL	0x230C	Control register for sink 3

Table 1: ADM-XRC-6T1 Reference Design for System Generator Registers (continued on next page)

Register	Offset	Description
SOURCE0_START_ADDR	0x3000	Start address for data to be output by source 0
SOURCE0_WORD_LIMIT	0x3004	Limit of 16 byte words of data to be output by source 0
SOURCE0_IRQ_LIMIT	0x3008	Number of 32 bit words of data sent before generating IRQ from source 0
SOURCE0_CONTROL	0x300C	Control register for source 0
SOURCE0_RATE_LIMIT	0x3010	Set output sample rate. Set to x to output a sample every x clock cycles. 0 or 1 outputs data every clock cycle.
SOURCE1_START_ADDR	0x3100	Start address for data to be output by source 1
SOURCE1_WORD_LIMIT	0x3104	Limit of 16 byte words of data to be output by source 1
SOURCE1_IRQ_LIMIT	0x3108	Number of 32 bit words of data sent before generating IRQ from source 1
SOURCE1_CONTROL	0x310C	Control register for source 1
SOURCE1_RATE_LIMIT	0x3110	Set output sample rate. Set to x to output a sample every x clock cycles. 0 or 1 outputs data every clock cycle.
SOURCE2_START_ADDR	0x3200	Start address for data to be output by source 2
SOURCE2_WORD_LIMIT	0x3204	Limit of 16 byte words of data to be output by source 2
SOURCE2_IRQ_LIMIT	0x3208	Number of 32 bit words of data sent before generating IRQ from source 2
SOURCE2_CONTROL	0x320C	Control register for source 2
SOURCE2_RATE_LIMIT	0x3210	Set output sample rate. Set to x to output a sample every x clock cycles. 0 or 1 outputs data every clock cycle.
SOURCE3_START_ADDR	0x3300	Start address for data to be output by source 3
SOURCE3_WORD_LIMIT	0x3304	Limit of 16 byte words of data to be output by source 3
SOURCE3_IRQ_LIMIT	0x3308	Number of 32 bit words of data sent before generating IRQ from source 3
SOURCE3_CONTROL	0x330C	Control register for source 3
SOURCE3_RATE_LIMIT	0x3310	Set output sample rate. Set to x to output a sample every x clock cycles. 0 or 1 outputs data every clock cycle.

Table 1: ADM-XRC-6T1 Reference Design for System Generator Registers

5.2 Register Details

5.3 Register Definitions

5.3.1 IRQ_STATUS - (0x0100)

31 8	7 4	3 0
SYSGEN_IRQ	SOURCE_IRQ	SINK_IRQ

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
SINK_IRQ	[3:0]	RW1C	0x0	Each bit set to 1 corresponds to an interrupt requested by the corresponding data sink Writing a 1 clears these bits to 0
SOURCE_IRQ	[7:4]	RW1C	0x0	Each bit set to 1 corresponds to an interrupt requested by the corresponding data source Writing a 1 clears these bits to 0
SYSGEN_IRQ	[31:8]	RW1C	0x000000	Each bit set to 1 corresponds to an interrupt requested from within the Sysgen Block Writing a 1 clears these bits to 0

Table 2: IRQ_STATUS Register Definition

Description:

Interrupt Status Register, Write to Clear

5.3.2 IRQ_ENABLE - (0x0104)

31 8	7 4	3 0
SYSGEN_IRQ	SOURCE_IRQ	SINK_IRQ

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
SINK_IRQ	[3:0]	RW	0x0	Enables IRQs from Data Sink 0-3
SOURCE_IRQ	[7:4]	RW	0x0	Enables IRQs from Data Source 0-3
SYSGEN_IRQ	[31:8]	RW	0x000000	Enables IQRs from Sysgen IRQ 0-23

Table 3: IRQ_ENABLE Register Definition

Description:

Interrupt Enable Register

5.3.3 SINKS_FLUSH_PACKET - (0x0108)

	3	0
	FLP	

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
FLUSH_PACKET	[3:0]	RW	0x0	set to flush data from data sink FIFO

Table 4: SINKS_FLUSH_PACKET Register Definition

Description:

Sink flush strobes

5.3.4 SINK0_CONTROL - (0x200C)

	3	2	1	0
	RST	CL	CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data Sink
CONTINUOUS (CO)	[1]	RW	0	Run data sink continuously
CLEAR (CL)	[2]	RW	0	Clear Data Sink
RST (RST)	[3]	RW	0	Reset Data Sink

Table 5: SINK0_CONTROL Register Definition

Description:

Control register for sink 0

5.3.5 SINK1_CONTROL - (0x210C)

	3	2	1	0
	RST	CL	CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data Sink
CONTINUOUS (CO)	[1]	RW	0	Run data sink continuously
CLEAR (CL)	[2]	RW	0	Clear Data Sink
RST (RST)	[3]	RW	0	Reset Data Sink

Table 6: SINK1_CONTROL Register Definition

Description:

Control register for sink 1

5.3.6 SINK2_CONTROL - (0x220C)

	3	2	1	0
	RST	CL	CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data Sink
CONTINUOUS (CO)	[1]	RW	0	Run data sink continuously
CLEAR (CL)	[2]	RW	0	Clear Data Sink
RST (RST)	[3]	RW	0	Reset Data Sink

Table 7: SINK2_CONTROL Register Definition

Description:

Control register for sink 2

5.3.7 SINK3_CONTROL - (0x230C)

	3	2	1	0
	RST	CL	CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data Sink
CONTINUOUS (CO)	[1]	RW	0	Run data sink continuously
CLEAR (CL)	[2]	RW	0	Clear Data Sink
RST (RST)	[3]	RW	0	Reset Data Sink

Table 8: SINK3_CONTROL Register Definition

Description:

Control register for sink 3

5.3.8 SOURCE0_CONTROL - (0x300C)

	3		1	0
	RST		CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data source
CONTINUOUS (CO)	[1]	RW	0	Run data source continuously
RST (RST)	[3]	RW	0	Reset Data Source

Table 9: SOURCE0_CONTROL Register Definition

Description:

Control register for source 0

5.3.9 SOURCE1_CONTROL - (0x310C)

	3		1	0
	RST		CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data source
CONTINUOUS (CO)	[1]	RW	0	Run data source continuously
RST (RST)	[3]	RW	0	Reset Data Source

Table 10: SOURCE1_CONTROL Register Definition

Description:

Control register for source 1

5.3.10 SOURCE2_CONTROL - (0x320C)

	3		1	0
	RST		CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data source
CONTINUOUS (CO)	[1]	RW	0	Run data source continuously
RST (RST)	[3]	RW	0	Reset Data Source

Table 11: SOURCE2_CONTROL Register Definition

Description:

Control register for source 2

5.3.11 SOURCE3_CONTROL - (0x330C)

	3		1	0
	RST		CO	ST

Field Definitions:

Field	Bit(s)	Mode	Init Value	Description
START (ST)	[0]	RW	0	Starts data source
CONTINUOUS (CO)	[1]	RW	0	Run data source continuously
RST (RST)	[3]	RW	0	Reset Data Source

Table 12: SOURCE3_CONTROL Register Definition

Description:

Control register for source 3

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Revision History:

Date	Revision	Nature of Change
23/05/11	4.1	Initial Release

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