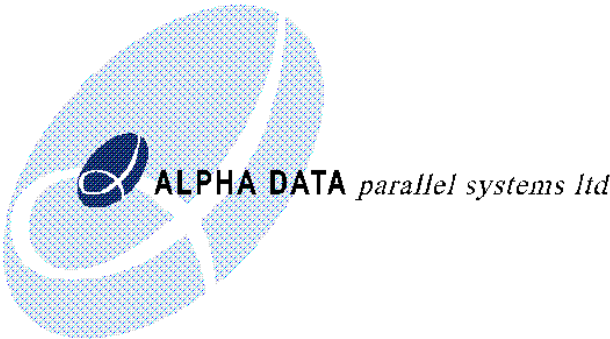


XRC Co-simulation Library v1.3





XRC Co-simulation Library for use with System Generator v6.2

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1 Introduction

The Alpha Data XRC Co-simulation Library is a Simulink Blockset designed for use in conjunction with Xilinx System Generator 6.2. This blockset enables System Generator Models to be Co-simulated using Alpha Data ADM-XRC-II-L, ADM-XRC-II, ADM-XRC-II-Pro-Lite (ADM-XPL) and ADM-XRC-II-Pro (ADM-XP) FPGA reconfigurable computing cards. The System Generator design methodology incorporating Co-simulation allows a very rapid move from Simulation in Simulink to Verification on Hardware. This design methodology can be used incrementally, with Co-simulated Hardware in the Loop modules used to accelerate the development and simulation of larger designs.

2 Installation Instructions

The XRC Co-simulation Library is provided as a zip file and a Matlab installation script:

```
xrc_cosim_blockset.zip  
setup_cosim.m
```

- 1) Open Matlab
- 2) Change Directory to where xrc_cosim_blockset.zip and setup_cosim.m have been downloaded.
- 3) Type setup_cosim
- 4) Quit Matlab

3 Using The Library

Once installed, board options for the ADM-XRC-II, ADM-XRC-II-Lite and ADM-XRC-II-Pro-Lite will appear in the Compilation->Hardware In The Loop menu of the System Generator GUI (accessed by double clicking on the System Generator token in your design). You can select the correct Alpha Data board and the correct FPGA specification from this GUI.

Now when Generate is pressed in the System Generator GUI, the VHDL is still created as normal, but afterwards, the Xilinx (and possibly 3rd party) synthesis tools are run to create a bitstream for the device and board selected. After this is finished, a new library containing a hardware cosimulation block will appear, as shown in figure 2.



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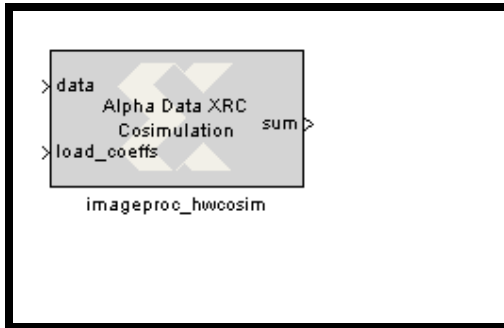


Figure 1: Hardware Cosimulation Block

This block can be inserted into a System Generator Simulink design in place of the model synthesized, for testing and verification or even as a simulation component, to accelerate the simulation of a higher level design. The block has 3 parameters, specifying the clock period, the generated bitstream and which Alpha Data board (if multiple boards are installed in the system) to use.