ADM-XRC-II

PCI Mezzanine Card

User Guide

Version 1.5

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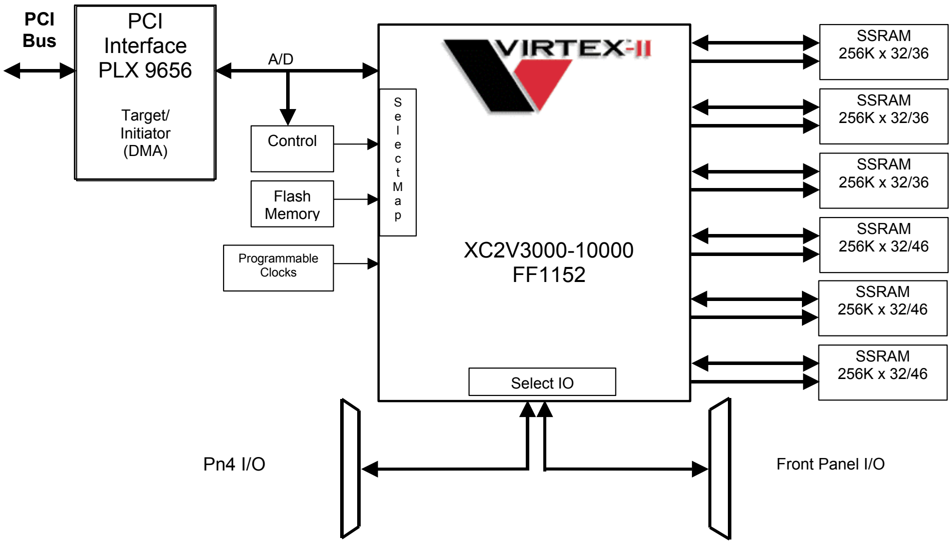
1. Introduction

The ADM-XRC-II is a high performance PCI Mezzanine Card (PMC) format device designed for supporting development of applications using the Virtex-II series of FPGA's from Xilinx.



1.1. Specifications

The ADM-XRC-II supports high performance PCI operation without the need to integrate proprietary cores into the FPGA. A PLX PCI9656 provides a rich set of PCI resources including two high-speed DMA.

- Physically conformant to IEEE P1386 Common Mezzanine Card standard
- High performance PCI and DMA controllers
- Local bus speeds of up to 66MHz
- Six banks of 256k/512kx32/36 ZBT SSRAM
- User clock programmable between 0.5MHz and 100MHz
- User front panel adapter with up to 146 free IO signals
- User rear panel PMC connector with 64 free IO signals
- Supports 3.3V and 5V PCI signalling levels (VI/O)

2. Installation

This chapter explains how to install the ADM-XRC-II onto a PMC motherboard.

2.1. Motherboard requirements

The ADM-XRC-II is a Universal PCI device and supports both 3.3V and 5V PCI signalling levels (VI/O).
The ADM-XRC-II must be installed in a PMC motherboard that supplies 3.3V power to the PMC connectors. Ensure that the motherboard satisfies this requirement before powering it up.

2.2. Handling instructions

Observe precautions for preventing damage to components by electrostatic discharge. Personnel handling the board should take SSD precautions.
Avoid flexing the board.

2.3. Installing the ADM-XRC-II onto a PMC motherboard

Note: This operation should not be performed while the PMC motherboard is powered up.
The ADM-XRC-II must be secured to the PMC motherboard using M2.5 screws in the four holes provided. The PMC bezel through which the I/O connector protrudes should be flush with the front panel of the PMC motherboard.

2.4. Installing the ADM-XRC-II if fitted to an ADC-PMC

The ADM-XRC-II can be supplied for use in standard PC systems fitted to an ADC-PMC carrier board. The ADC-PMC can support up to two ADC-PMC cards whilst maintaining host PC PCI compatibility. If you are using a ADC-PMC64 refer to the supplied documentation for information on jumper settings. All that is required for installation is a 5V PCI slot that has enough space to accommodate the full-length card.

It should be noted that the ADC-PMC uses a standard bridge to provide a secondary PCI bus for the ADM-XRC-II and that some older BIOS code does not set up these devices correctly. Please ensure you have the latest version of BIOS appropriate for your machine. The ADC-PMC requires only 5V from the host PC.

3. Board Overview

The ADM-XRC-II PMC provides an easy way to achieve PCI performance without the need to develop or incorporate PCI cores into the FPGA design. The benefit provided by this architecture means faster development time and reduced cost in evaluating and testing FPGA applications.

The XRC effectively connects the FPGA directly to the local bus of the PCI9656 to enable two main modes of operation, slave and master. A Complex Programmable Logic Device or CPLD also resides on the local bus and manages access to resources such as flash, SelectMAP and the clock generator.

In direct slave mode, the XRC is a target on the PCI bus for read and write transactions and these are translated into local bus cycles initiated by the PCI9656.

In direct master mode, the FPGA can request control over the local bus and initiate transactions to the PLX. These transactions are translated by the PLX into PCI master operations to read or write another PCI target.

In both master and slave modes of operation the FPGA can use burst capability to boost performance and achieve very high data transfer rates. In most PC systems, 240MB/s is achievable but this can vary depending on the quality of the PC chipset and the ability of the BIOS to configure PCI devices correctly.

4. PCI Bus Interface

The PCI bus is implemented in a PLX PCI9656 and is configured with settings as described later in this document to simplify the integration of user applications in the FPGA.

The PCI configuration space of the ADM-XRC-II is shown below.

Config. Offset	31 24	23 16	15 8	7 0
00	Device ID (0042) (9656)		Vendor ID (4144) (10B5)	
04	Status		Command	
08	Class Code			RevisionID
0C	BIST	HeaderType	Lat. Timer	Cache Line
10	PCI BAR0 (PLX Internal Registers/Memory)			
14	PCI BAR1 (PLX Internal Registers/IO)			
18	PCI BAR2 (Local Bus FPGA)			
1C	PCI BAR3 (Local Bus Control/Flash/SelectMap)			
20	PCI BAR4 (Not used)			
24	PCI BAR5 (Not used)			
28	Card Bus CIS Pointer(Not used)			
2C	Subsystem ID		Subsystem Vendor ID	
30	PCI Base Address for Local Expansion ROM			
34	Reserved			
38	Reserved			
3C	Max Lat	Min Gnt	Int. Pin	Int. Line

The PCI9656 uses the first two Bar’s to provide access to its internal registers both via memory accesses and I/O accesses. Either BAR may be used by the host.

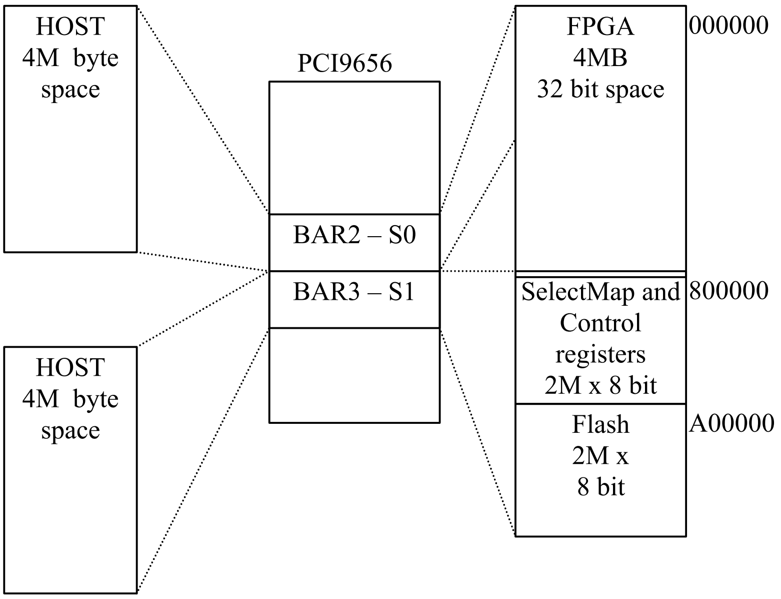
BAR 2 provides access to a 4Mbyte space for use by the FPGA and must be accessed only when a valid FPGA configuration is loaded that can respond correctly to local bus access.

BAR 3 provides access to the local control registers and the flash memory.

5. ADM-XRC-II Local Bus Architecture

It is useful to refer to the PLX PCI9656 user manual for information on the operation of the local bus and how address spaces map to the BAR's in PCI configuration space. The first two BAR's decode memory and I/O ranges for the PCI9656 internal registers.

There are a further two BAR's (at offsets 0x18 and 0x1C) that map the two main local bus address spaces, S0 and S1. In the XRC, S0 is an 4Mbyte memory address space, 32-bits wide and is available for the user to access the FPGA . S1 maps in a 4Mbyte memory address space, 8 bits wide for access to the control registers, flash and FPGA SelectMap port.



The PCI9656 can be programmed to support 8, 16 or 32 bit local bus widths and this feature is used to match with the device widths fitted on the XRC. Other than programming the BAR's with values determined by the host system, no other programming of the PCI9656 is required in order to access the local bus registers and devices.

5.1. Characteristics of Address Spaces

The XRC maps two PCI BAR spaces to the local bus and are specified to operate differently as shown below.

Space	Size	Width	Burst	Prefetch	Burst Term	Local Offset
S0	4MB	32	yes	no	yes	0x00000000
S1	4MB	8	yes	no	yes	0x00800000

From the PCI side of the PCI9656, transfers to either space may be 8, 16 or 32-bit in width and of any length. The PCI9656 breaks up transfers to suit the address space on the local bus whilst respecting the characteristics outlined above.

5.2. Local Control Registers

The local bus control registers are implemented in a CPLD attached to the PCI9656 local bus. The map of these registers is shown below.

S1+offset	Write	Read
0	FCON	FSTAT
1	CCON	CSTAT
2	IMSET	IMSTAT
3	IMCLR	IMSTAT
4	ICON	ISTAT
5	PCON	PSTAT
6	MODE	MODE
7	FlashPage	FlashPage
8-15	SelectMap	SelectMap

Registers that are not implemented are marked Must Be Zero (MBZ) and Read As Don't Care (RAX). The same applies for bits within implemented registers that are not used or reserved.

5.2.1. FCON Register

The FPGA can be configured by the host system using the SelectMap port on the target device. Before this can be achieved, the FPGA must be initialised to an erased state. Asserting PROG and then releasing it will start the initialisation process. The INIT bit is only valid whilst the device is not configured, indicated by a zero in DONE. After configuration, the INIT pin becomes a user I/O pin and has no further function on the ADM-XRC-II. In this case the place and route program sets the INIT pin to an input with a weak pull down thus resulting in INIT appearing set.

	7	6	5	4	3	2	1	0	
FCON	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	INIT	PROG	W
FSTAT	RAX	RAX	RAX	RAX	RAX	DONE	INIT	PROG	R

FCON Function (W0/1 is write value, R is when read)

PROG W0 - Release PROGRAM to the FPGA
W1 - Asserts PROGRAM pin on the target FPGA
RX - Indicates state of FCON[PROG]

INIT W0 - Has no effect on FPGA INIT pin
W1 - Asserts INIT pin to FPGA to postpone configuration
R0 - FPGA has no error
R1 - FPGA has asserted INIT

DONE R0 - FPGA is not configured or is being configured
R1 - FPGA is successfully configured

5.2.2. CCON Register

The CCON register controls access to the ICS9161A clock generator. The range of frequencies supported is between 25 and 66 MHz. Although the XRC can operate at frequencies less than 25MHz, the CLKDLL circuits in the FPGA will not. The maximum frequency of the PCI9656 local bus is 66MHZ. Refer to the ICS9161A data sheet for further information on determining clock generator settings.

	7	6	5	4	3	2	1	0	
CCON	MBZ	MBZ	MBZ	MBZ	INTCLK	FEATCLK	DATA/S1	CLK/S0	W
CSTAT	RAX	RAX	RAX	SERERR	INTCLK	FEATCLK	DATA/S1	CLK/S0	R

CLK	Drives clock signal to ICS9161 Determines S0 when static
DATA	Drives data signal to ICS9161 Determines S1 when static
FEATCLK	Do not use
INTCLK	Do not use

The ICS9161 is programmed using CLK and DATA bits to form manchester encoded sequences. Each sequence consists of a 5 bit unlock preamble followed by a 24 bit data word all of which must be programmed within 10ms from the start of the first bit. If programming is not completed within this time, the ICS9161 will assert SERERR and ignore the remainder of the sequence. When the ICS9161 is not being programmed, S1 and S0 select the internal VCLK programming register.

5.2.3. ICON Registers

The ICON registers consist of a mask register and an interrupt status register. The mask register can be set or cleared by writing to IMSET or IMCLR with a bit mask. The XRC only supports one interrupt from the local bus and is masked, set or cleared using bit 0. On reset the mask bits are set disabling local bus interrupts.

	7	6	5	4	3	2	1	0	
IMSET	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	FINTM	W
IMCLR	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	FINTM	W
IMSTAT	RAX	RAX	RAX	RAX	RAX	RAX	RAX	FINTM	R

The ICON register contains the status of the interrupt from the FPGA. This bit can be read independently of the state of the FINTM mask bit.

The method used to clear FINT in the ISTAT register depends on the interrupt mode selected by IMODE (MODE [0]).

- With edge-triggered interrupts, writing the FINT bit in ICON clears the corresponding bit in ISTAT.
- For level sensitive interrupts, FINT can only be cleared by removing the interrupting source in the FPGA.

	7	6	5	4	3	2	1	0	
ICON	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	FINT	W
ISTAT	RAX	RAX	RAX	RAX	RAX	RAX	RAX	FINT	R

5.2.4. PSTAT Register

The PSTAT register presents information about the power supply to the Virtex device. The XRC generates power for the FPGA core from 5V, using a switch mode supply circuit that outputs two signals to indicate over-temperature and accuracy.

	7	6	5	4	3	2	1	0	
PSTAT	RAX	RAX	RAX	RAX	RAX	RAX	PTEMP	PGOOD	R

PGOOD	0 => PSU is out of range
	1 => PSU is within +/- 10%
PTEMP	0 => PSU has shutdown (thermal detect)
	1 => PSU is within operating range

5.2.5. MODE Register

The MODE register contains fields that allow the additional functionality of operations to be specified.

	7	6	5	4	3	2	1	0	
MODE	MBZ	MBZ	MBZ	MBZ	MBZ	MBZ	BREV	IMODE	W
MODE	RAX	RAX	RAX	RAX	RAX	RAX	BREV	IMODE	R

IMODE 0 => Edge triggered interrupt mode
1 => Level sensitive interrupt mode
BREV 0 => SelectMAP port LSB is DIN/D0
1 => SelectMAP port MSB is DIN/D0

5.2.6. Flash_Page Register

The Flash Page register is used to provide the upper flash address bits. The flash page size is set at 2M bytes and the upper address bits are provided from the register as follows :-

	7	6	5	4	3	2	1	0	
Flashpage	Configuration Data Byte								W

5.2.7. SelectMAP Register

The XRC supports only SelectMAP download of configuration data to the Virtex FPGA. The SelectMAP register is a write only port (in the current XRC) that is written with configuration information. The mapping of this port is determined by the BREV bit in the MODE register.

	7	6	5	4	3	2	1	0	
SelectMap	Configuration Data Byte								W

NOTE. Do not write to the SelectMAP register whilst DONE is set.

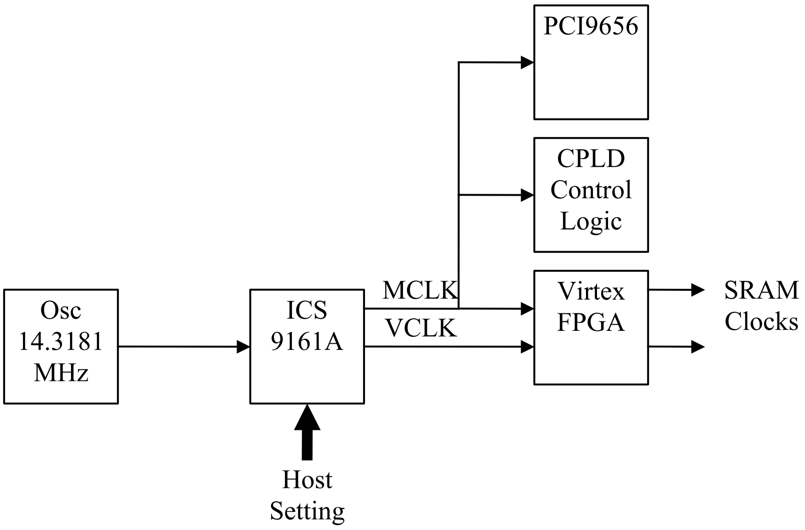
FPGA Operation

The following sections describe the operation of the FPGA in terms of the resources that are available. Where pin numbers are not mentioned, these can be found in the constraints file for the various Virtex II devices, supplied with the SDK. Please refer to the installation directory for examples of working designs and guidelines.

5.3. Clock Distribution

The XRC uses the PLX PCI9656 local bus to provide a synchronous data transfer interface and all devices attached to the PCI9656 run at the local bus clock rate.
The MCLK output from the ICS9161 provides the local bus clock and by default runs at 32.5MHz. The VCLK output can be determined by three registers in the ICS9161, selected by the S1/S0 bits in the CCON register. It is

recommended that alterations to VCLK use REG1 or REG2 to set the new value so that on reset the VCLK output selects REG0 when S1/S0 are reset.



5.4. Input Clocks

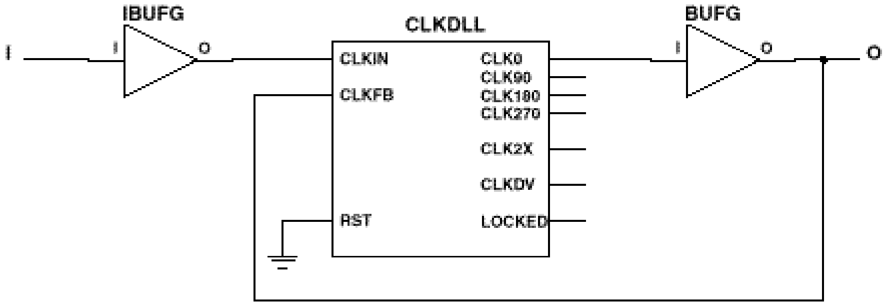
There are two primary clock inputs to the FPGA, both from the programmable clock generator. The VCLK signal from the clock generator is used only by the FPGA. It is therefore free for use by logic in the FPGA.

The MCLK signal from the clock generator is the local bus clock, used by the FPGA, PLX PCI9656 and a support CPLD.

Both MCLK and VCLK can be programmed between 400kHz and 100MHz.

A restriction on MCLK is that it must not exceed 66MHz,the maximum speed of the PCI9656, and should not be lower than 25MHz for reliable CLKDLL operation.

MCLK is input to the FPGA on GCK7 (pin AG18) and should be used to drive a Virtex CLKDLL circuit which aligns the internal FPGA clock to the local bus clock. The circuit below demonstrates how to align the internal clock of the FPGA to the local bus clock. The output of the BUFG is available to all flip-flops in the design.



VCLK is input to the FPGA on GCK1 (pin AF18) and can be used for any purpose within the FPGA.

5.5. Output Clocks

The FPGA is responsible for providing clocks to the SRAM's and also for aligning its internal global clock with the local bus clock. To do this requires the use of Virtex DCM's that are specifically designed for the purpose of minimising skew between external and internal clock domains.

The SRAM's are split into two banks of three – each bank of three has its own FPGA clock output and feedback pin to allow deskewing within the FPGA. Further details of SRAM clocking are provided in section 5.8.

5.6. Local Bus

The local bus of the ADM-XRC-II uses the PCI9656 to provide a non-multiplexed address and data capability with synchronous speeds of up to 66MHz, independent of PCI operation. Whilst the local bus is capable of achieving near PCI performance, it is much simpler to interface with than PCI. The ADM-XRC-II routes most of the local bus signals to the FPGA and devotes an entire address space to the FPGA.
The signals provided are :-

Signal	Active	Direction	Purpose
LA[31:2]	high	IN	Address
LBE[3:0}	low	IN	Address/byte enables
LD[31:0]	high	BIDIR	Data Bus
LWRITE	high	IN	Write cycle when true, read when false
LBLASTL	low	IN	End of burst
LADSL	low	IN	Address / data start
LBTERML	low	OUT/TRI	Burst terminate
LREADYIL	low	OUT/TRI	Accepts/completes data transfer
LDREQL[1:0]	low	OUT	Request DMA transfer
LDACKL[1:0]	low	IN	DMA transfer acknowledge
LEOTL[1:0]	low	OUT	Terminate current DMA transfer
LINTIL	low	OUT	Interrupt (via CPLD)
FHOLD	high	OUT	Reserved for future use
FHOLDA	high	IN	Reserved for future use
LRESETOL	low	IN	Reset from PLX and PCI
LCLKA	high	IN	Local bus clock (VCLK from ICS9161)

The local bus provides 8Mbytes of address space for the FPGA to use for whatever purpose is desired by the application. LA[23]=0 should be used to determine when the FPGA is being accessed.

Example Verilog code demonstrates how to interface to the local bus and provide access to the SSRAM's for test purposes. User applications can define how the address space allocated to the FPGA is mapped to the local bus and may or may not provide access to the SRAM memory.

5.7. Synchronous SRAM

The four banks of synchronous SRAM are identical in device type and FPGA interface. The devices fitted as pipelined ZBT parts organised as 256Kx32/36 bits each.
The pins are allocated to support synchronous burst or ZBT SRAM and each bank provides the following interface.

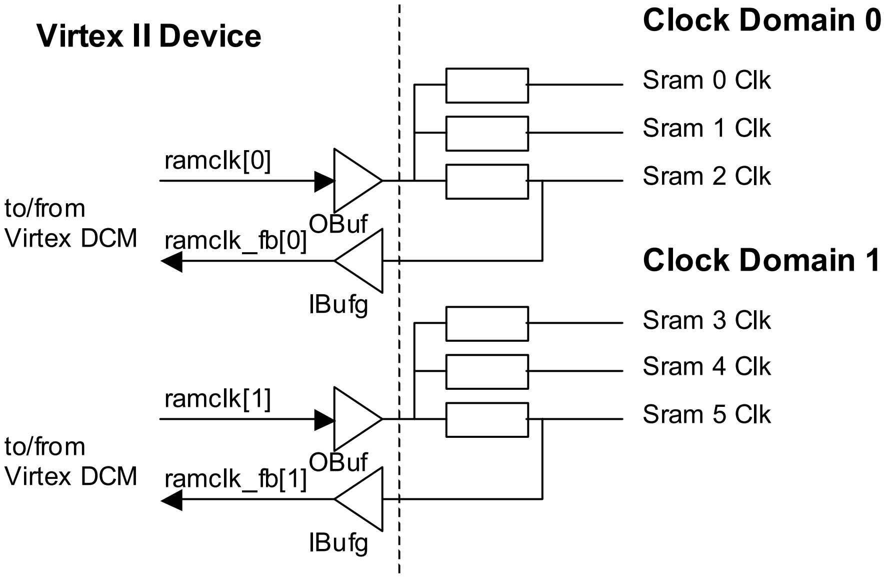
FPGA Pin	Active	Type	Function
RD**n**[36:0]	high	Bidir	Data Bus
RA**n**[19:0]	high	OUT	Address Bus
RC**n**[3:0]	low	OUT	Byte enables
RC**n**[4]	low	OUT	Global write enable
RC**n**[5]	low	OUT	Chip enable
RC**n**[6]	low	OUT	ADV (advance) function
RC**n**[7]	low	OUT	Output enable
RCn[8]	low	OUT	CKE - clock enable

Where **n** = 0,1,2,3,4,5. Therefore, SRAM 0 is controlled by the three bus ports RD0[36:0], RA0[19:0] and RC0[8:0] and these are names used to constrain the pins in the user constraints file or UCF.

5.8. Clock pins

The six banks of SRAM are divided into two clock domains. Each SRAM clock domain has its own pin routed from the FPGA.

ramclk[0]	OUT	Clock to SRAM 0, SRAM 1, SRAM 2
ramclk[1]	OUT	Clock to SRAM 3, SRAM 4, SRAM 5
ramclk_fb[0]	INPUT	Clock feedback for ramclk[0]
ramclk_fb[1]	INPUT	Clock feedback for ramclk[1]

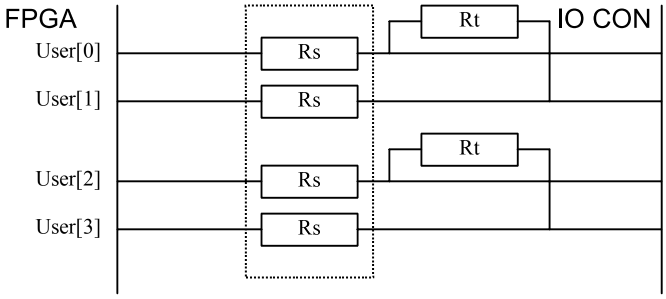


5.9. User I/O Configuration

The ADM-XRC-II is fitted with and IO adapter to provide user I/O capability via the front panel. This allows many different IO connectors and standards to be easily supported. Currently the following IO adapter cards are available

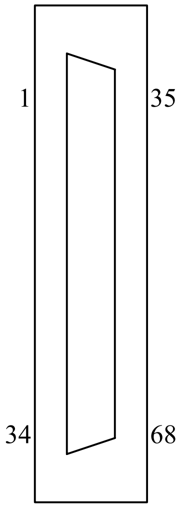
5.9.1. User I/O XRM IO34 Front Panel Variant

There are 34 I/O signals available on the front panel connector and these can be used individually or in pairs. All of these signals are from one bank of the FPGA and are provided with a VCCo supply voltage of 2.5V or 3.3V selected by JP1. A link on pins 2-3 selects 2.5V whilst a link on pins 1-2 select 3.3V. Each pair of I/O signals is routed as shown below.



The default manufacturing option is Rs=0R and Rt not fitted. Other options are available. Rs can be used to provide series damping in point to point applications but for LVDS is 0R. Rt is required for LVDS inputs to provide the termination voltage from the line current.

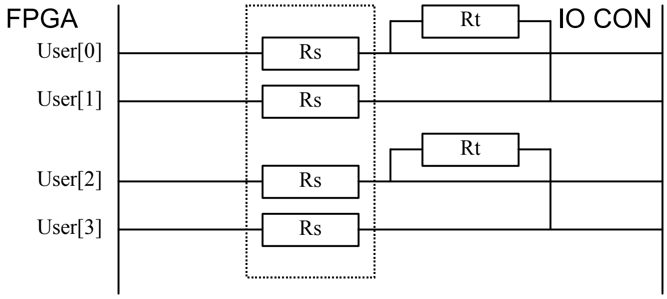
User I/O is presented on a 68 way miniature D connector (of SCSI-2 style) with interleaved signal and ground pairs as shown below. All of the user pins are routed in pairs to suit the differential assignments of the FPGA e.g. user[1:0] are the first up to user[33:32].



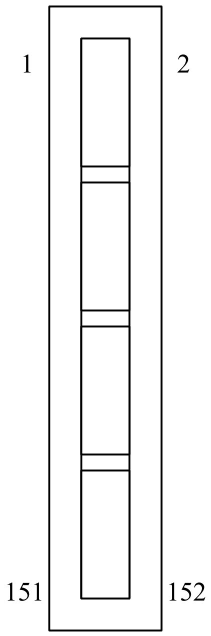
Signal	Pin	Pin	Signal
All GND	1	35	USER[0]
	2	36	USER[1]
	3	37	USER[2]
	4	38	USER[3]
	5	39	USER[4]
	6	40	USER[5]
	7	41	USER[6]
	8	42	USER[7]
	9	42	USER[8]
	10	44	USER[9]
	11	45	USER[10]
	12	46	USER[11]
	13	47	USER[12]
	14	48	USER[13]
	15	49	USER[14]
	16	50	USER[15]
	17	51	USER[16]
	18	52	USER[17]
	19	53	USER[18]
	20	54	USER[19]
	21	55	USER[20]
	22	56	USER[21]
	23	57	USER[22]
	24	58	USER[23]
	25	59	USER[24]
	26	60	USER[25]
	27	61	USER[26]
	28	62	USER[27]
	29	63	USER[28]
	30	64	USER[29]
	31	65	USER[30]
	32	66	USER[31]
	33	67	USER[32] -CLK
	34	68	USER[33] -CLK

5.9.2. User I/O XRM IO146 Panel Variant – Rev2.0

There are 146 I/O signals available on the front panel connector and these can be used individually or in pairs. Each pair of I/O signals is routed as shown below.



The default manufacturing option is Rs=0R and Rt not fitted. Other options are available. Rs can be used to provide series damping in point to point applications but for LVDS is 0R. Rt is required for LVDS inputs to provide the termination voltage from the line current.



Pin numbering looking into front of XRM IO146 connector

Pin	Function	UCF name	Term Res	V II Pin	Pin	Function	UCF name	Term Res	V II Pin
1	Data[0] +ve	User[0]	R1	B3	2	Data[1] +ve	User[2]	R4	C9
3	Data[0] -ve	User[1]	-	C2	4	Data[1] -ve	User[3]	-	D9
5	Data[2] +ve	User[4]	R3	B5	5	Data[3] +ve	User[6]	R2	E9
7	Data[2] -ve	User[5]	-	B4	6	Data[3] -ve	User[7]	-	E8
9	Data[4] +ve	User[8]	R5	C6	10	Data[5] +ve	User[10]	R6	B10
11	Data[4] -ve	User[9]	-	D6	12	Data[5] -ve	User[11]	-	B9
13	Data[6] +ve	User[12]	R7	J10	14	Data[7] +ve	User[14]	R8	D11
15	Data[6] -ve	User[13]	-	H11	16	Data[7] -ve	User[15]	-	D10
17	Data[8] +ve	User[16]	R9	F8	18	Data[9] +ve	User[18]	R10	G11
19	Data[8] -ve	User[17]	-	F9	20	Data[9] -ve	User[19]	-	G10
21	Data[10]+ve	User[20]	R11	B7	22	Data[11] +ve	User[22]	R12	H9
23	Data[10] -ve	User[21]	-	B6	24	Data[11] -ve	User[23]	-	H10
25	Data[12]+ve	User[24]	R14	C8	26	Data[13] +ve	User[26]	R15	H12
27	Data[12] -ve	User[25]	-	C7	28	Data[13] -ve	User[27]	-	H13
29	Data[14]+ve	User[28]	R16	A5	30	Data[15] +ve	User[30]	R17	J11
31	Data[14] -ve	User[29]	-	A4	32	Data[15] -ve	User[31]	-	J12
33	Single 0	User[34]	N/a	A9	34	Clock[0] +ve	User[32]	R64	H16
35	Single 1	User[35]	N/a	F13	36	Clock[0] -ve	User[33]	-	H17
37	+5V fused				38	Single 2	User[36]	N/a	C16

Pin	Function	UCF name	Term Res	V II Pin	Pin	Function	UCF name	Term Res	V II Pin
39	Data[16] +ve	User[40]	R19	A7	40	Data[17] +ve	User[42]	R20	K12
41	Data[16] -ve	User[41]	-	A6	42	Data[17] -ve	User[43]	-	J13
43	Data[18] +ve	User[44]	R23	A12	44	Data[19] +ve	User[46]	R22	C12
45	Data[18] -ve	User[45]	-	A11	46	Data[19] -ve	User[47]	-	C11
47	Data[20] +ve	User[48]	R25	B12	48	Data[21] +ve	User[50]	R24	B14
49	Data[20] -ve	User[49]	-	B11	50	Data[21] -ve	User[51]	-	B13
51	Data[22] +ve	User[52]	R27	D13	52	Data[23] +ve	User[54]	R26	G13
53	Data[22] -ve	User[53]	-	D12	54	Data[23] -ve	User[55]	-	G12
55	Data[24] +ve	User[56]	R29	E14	56	Data[25] +ve	User[58]	R28	J14
57	Data[24] -ve	User[57]	-	E13	58	Data[25] -ve	User[59]	-	J15
59	Data[26] +ve	User[60]	R37	K13	60	Data[27] +ve	User[62]	R30	C14
61	Data[26] -ve	User[61]	-	K14	62	Data[27] -ve	User[63]	-	C13
63	Data[28] +ve	User[64]	R41	K15	64	Data[29] +ve	User[66]	R38	H14
65	Data[28] -ve	User[65]	-	K16	66	Data[29] -ve	User[67]	-	H15
67	Data[30] +ve	User[68]	R44	G17	68	Data[31] +ve	User[70]	R42	F17
69	Data[30] -ve	User[69]	-	G16	70	Data[31] -ve	User[71]	-	F16
71	Single 3	User[37]	N/a	G20	72	Clock[1] +ve	User[72]	R67	E16
73	Single 4	User[38]	N/a	A28	74	Clock[1] –ve	User[73]	-	E17
75	+5V fused				76	Single 5	User[39]	N/a	G15

Pin	Function	UCF name	Term Res	V II Pin	Pin	Function	UCF name	Term Res	V II Pin
77	Data[32] +ve	User[74]	R48	F19	78	Data[33] +ve	User[76]	R45	G19
79	Data[32] -ve	User[75]	-	F18	80	Data[33] -ve	User[77	-	G18
81	Data[34] +ve	User[78]	R50	K19	82	Data[35] +ve	User[80]	R49	K22
83	Data[34] -ve	User[79]	-	J20	84	Data[35] -ve	User[81]	-	K23
85	Data[36] +ve	User[82]	R52	A24	86	Data[37] +ve	User[84]	R51	H20
87	Data[36] -ve	User[83]	-	A23	88	Data[37] -ve	User[85]	-	H21
89	Data[38] +ve	User[86]	R54	A26	90	Data[39] +ve	User[88]	R53	J21
91	Data[38] -ve	User[87]	-	B27	92	Data[39] -ve	User[89]	-	J22
93	Data[40] +ve	User[90]	R56	A31	94	Data[41] +ve	User[92]	R55	D21
95	Data[40] -ve	User[91]	-	A30	96	Data[41] -ve	User[93]	-	D20
97	Data[42] +ve	User[94]	R58	H24	98	Data[43] +ve	User[96]	R57	E22
99	Data[42] -ve	User[95]	-	H25	100	Data[43] -ve	User[97]	-	E21
101	Data[44] +ve	User[98]	R60	G26	102	Data[45] +ve	User[100]	R59	B22
103	Data[44] -ve	User[99]	-	H26	104	Data[45] -ve	User[101]	-	B21
105	Data[46] +ve	User[102]	R62	F27	106	Data[47] +ve	User[104]	R63	D23
107	Data[46] -ve	User[103]	-	E26	108	Data[47] -ve	User[105]	-	D22
109	Single 6	User[108]	N/a	D17	110	Clock[2] +ve	User[106]	R46	J18
111	Single 7	User[109]	N/a	D18	112	Clock[2] -ve	User[107]	-	K18
113	+5V fused				114	+5V fused			

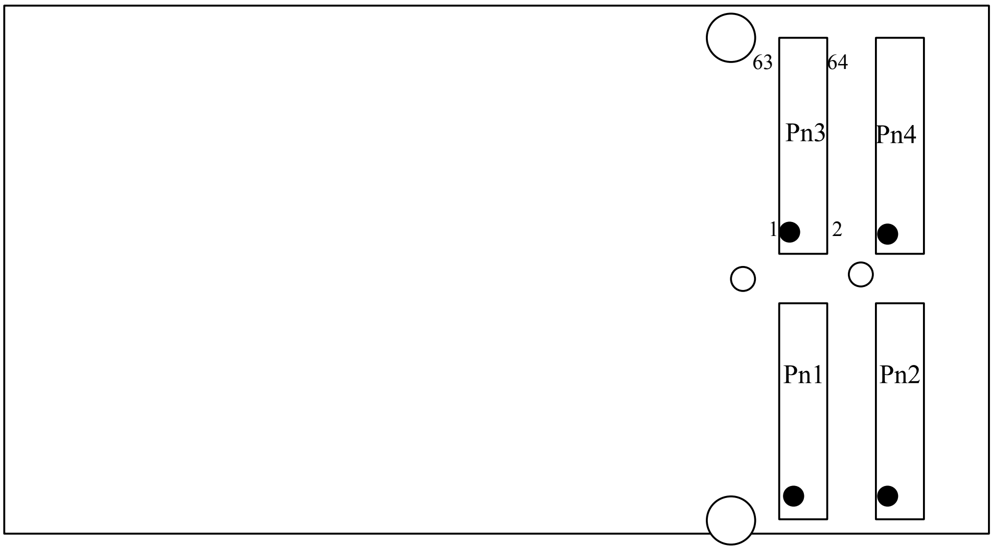
Pin	Function	UCF name	Tem Res	V II Pin	Pin	Function	UCF name	Tem Res	V II Pin
115	Data[48] +ve	User[110]	R65	J23	116	Data[49] +ve	User[112]	R61	H22
117	Data[48] -ve	User[111]	-	J24	118	Data[49] -ve	User[113]	-	H23
119	Data[50] +ve	User[114]	R68	E27	120	Data[51] +ve	User[116]	R66	C23
121	Data[50] -ve	User[115]	-	E28	122	Data[51] -ve	User[117]	-	C22
123	Data[52] +ve	User[118]	R71	C29	124	Data[53] +ve	User[120]	R69	B24
125	Data[52] -ve	User[119]	-	D29	126	Data[53] -ve	User[121]	-	B23
127	Data[54] +ve	User[122]	R73	G23	128	Data[55] +ve	User[124]	R72	F24
129	Data[54] -ve	User[123]	-	G22	130	Data[55] -ve	User[125]	-	F23
131	Data[56] +ve	User[126]	R77	B31	132	Data[57] +ve	User[128]	R74	D24
133	Data[56] -ve	User[127]	-	B30	134	Data[57] -ve	User[129]	-	C24
135	Data[58] +ve	User[130]	R79	D27	136	Data[59] +ve	User[132]	R78	G25
137	Data[58] -ve	User[131]	-	C26	138	Data[59] -ve	User[133]	-	G24
139	Data[60] +ve	User[134]	R81	B29	140	Data[61] +ve	User[136]	R80	D26
141	Data[60] -ve	User[135]	-	B28	142	Data[61] -ve	User[137]	-	D25
143	Data[62] +ve	User[138]	R84	C33	144	Data[63] +ve	User[140]	R21	K20
145	Data[62] -ve	User[139]	-	B32	146	Data[63] -ve	User[141]	-	K21
147	Single 8	User[144]	N/a	C18	148	Clock[3] +ve	User[142]	R47	E18
149	Single 9	User[145]	N/a	F22	150	Clock[3] -ve	User[143]	-	E19
151	+5V fused				152	+5V fused			

Notes

1) Data[] signals can be used for differential Pairs or single ended signals
2) Clock[] can be used for differential clocks or single ended clock signals
3) XRM I0146 connector – AMP/TYCO 767044-4 152 pin Mictor Receptacle
4) Suggested mating part – AMP/TYCO 767007-1 152 pin Mictor Plug or similar

5.10. User I/O PMC Pn4

User I/O is presented on the User Connector Pn4 via a standard 64-way PMC connector. This should be routed via a suitable CMC compliant motherboard to an external I/O adapter.



Signal	Pn4 Pin	Pn4 Pin	Signal
REARIO[1]	1	2	REARIO[0]
REARIO[3]	3	4	REARIO[2]
REARIO[5]	5	6	REARIO[4]
REARIO[7]	7	8	REARIO[6]
REARIO[9]	9	10	REARIO[8]
REARIO[11]	11	12	REARIO[10]
REARIO[13]	13	14	REARIO[12]
REARIO[15]	15	16	REARIO[14]
REARIO[17]	17	18	REARIO[16]
REARIO[19]	19	20	REARIO[18]
REARIO[21]	21	22	REARIO[20]
REARIO[23]	23	24	REARIO[22]
REARIO[25]	25	26	REARIO[24]
REARIO[27]	27	28	REARIO[26]
REARIO[29]	29	30	REARIO[28]
REARIO[31]	31	32	REARIO[30]
REARIO[33]	33	34	REARIO[32]
REARIO[35]	35	36	REARIO[34]
REARIO[37]	37	38	REARIO[36]
REARIO[39]	39	40	REARIO[38]
REARIO[41]	41	42	REARIO[40]
REARIO[43]	43	44	REARIO[42]
REARIO[45]	45	46	REARIO[44]
REARIO[47]	47	48	REARIO[46]
REARIO[49]	49	50	REARIO[48]
REARIO[51]	51	52	REARIO[50]
REARIO[53]	53	54	REARIO[52]
REARIO[55]	55	56	REARIO[54]
REARIO[57]	57	58	REARIO[56]
REARIO[59]	59	60	REARIO[58]
REARIO[61]	61	62	REARIO[60]
REARIO[63]	63	64	REARIO[62]

6. Configuring the FPGA

The Virtex FPGA family support a mode of configuration referred to as SelectMAP. The ADM-XRC-II uses the local bus clock to synchronise byte loading through the SelectMAP interface and is thus limited to a maximum of 66Mbytes/sec.

6.1. SelectMAP Operation

Before the FPGA can be configured using SelectMAP, the FPGA must be in a state where it is ready to accept data. This can be confirmed by the following process: -

1. Assert PROG and INIT, hold for 20 usec.
2. Release PROG and INIT, wait for 50usec
3. Check that INIT is not set.

If INIT is clear then configuration can proceed.

Configuration is a simple process and requires the entire bitstream to be written to the SelectMAP register. At the end of the process, DONE should be high. If DONE is not high and INIT is set then an error has occurred and will probably be due to an invalid bitstream. Note that INIT is not valid when DONE is set as it becomes a user I/O after configuration and is pulled low (active) by default.

6.2. Bitstream Issues

The bitstream produced by the **bitgen** program is stored in a **design.bit** file and is suitable for use with the download cables produced by Xilinx. The driver for the ADM-XRC-II loads this file and determines the location of the binary bitstream data within it. This data is not suitable for writing directly to the Selectman registers as it is bit reversed. The driver performs this bit reversal on each byte before download to the FPGA.

Files generated by the **promgen** program and stored in **mcs** format for example are not bit reversed but the resulting file is around three times larger than the binary **design.bit** file.

7. Interrupts

The PCI9656 can provide a number of interrupts from internal sources as well as from the local bus. The FPGA can interrupt the host system by asserting the LINTIL (active low) signal and keeping it asserted until the source of the interrupt is cleared. See the ICON registers on how to mask and respond to local bus interrupts.

8. Flash Memory

The flash memory fitted is 16 M Bytes of Intel Strata Flash – part No 28F128J3A and is paged into a 2 Mbyte region accessible on the Local Bus. Refer to section 5.2 for further information on the flash paging register

The ADM-XRC-II is capable of loading the FPGA from flash on power up or reset and will load the bitstream from the main memory section starting at 0x8001. This is to avoid any problem with the boot block which, if locked out, cannot be unlocked without removing the flash device from the PCB. The byte at location 0x8000 should be programmed with bit 0 = 0 (all other bits are ignored) to enable the load sequence otherwise the assumption is the flash is blank and should not be used.

9. PLX PCI9656 Initialisation

The PCI9656 is configured at power-up and reset by a serial EEPROM attached to it. This device is configured at the factory with settings to suit the standard operation of the ADM-XRC-II. For the values in the EEPROM, see the following chapter.

After reset, the PCI9656 loads initial settings for PCI and other registers from the EEPROM. The following sections show the PCI9656 registers after booting on a system with a PCI BIOS.

9.1. PCI Registers

The PCI9656 PCI registers are accessed in PCI configuration space primarily during system boot to configure resources requested by the ADM-XRC-II.

The main points to note are that the device and vendor ID's are 9656/10B5 and the command register is set for memory and I/O access.

BAR0(10h) is allocated to 32 bit memory space and is used for access to all of the PCI9656 control registers. BAR1(14h) is allocated to I/O space and is used for the same purpose as BAR1.

BAR2 defines the PCI9656 Local Bus address range Space 0 (S0) and is allocated to 32 bit memory space. BAR3 maps a similar amount to BAR2 and is used for access to Space 1 (S1).

It is important to note that as far as PCI space is concerned, there is no difference between S0 and S1. The Local Bus registers define the operation of these spaces.

9.2. Local Configuration Registers

The PCI9656 Local Bus provides two main address spaces through which accesses to local bus resources can be made. As described earlier, S0 is a 4Mbyte space that is 32 bits wide, allocated to the FPGA. S1 is also a 4Mbyte space and is allocated to the flash prom and control registers. The Local Configuration registers are shown below in summary with more detailed descriptions following them.

9.2.1. Mode/Arbitration Register

The Mode/Arbitration Register is usually set by the EEPROM initialisation and left unaltered after boot.

The **PCI Rev 2.1 Mode** pin sets the behaviour of the PCI9656 to conform to PCI revision 2.1 with regard to posted transactions.

The **PCI Read No Write Mode** bit is set to cause PCI writes to the PCI9656 to retry whilst a posted read is pending. This is a known workaround in REV 3 silicon.

9.2.2. Big/Little Endian Descriptor Register

This register can be used to force big endian mode for various transfers. The ADM-XRC-II does not perform any endian conversions by default.

9.2.3. Region 0 Descriptor

The Region 0 Descriptor describes the attributes of Local Bus Space 0. It can be seen that 32 bit local bus width is selected and that ready must be generated by the target space. In this case, Space 0 is allocated to the FPGA so all accesses to Space 0 must be acknowledged by the FPGA.
The BTERM bit is set which means that bursts of greater the four LWORD's are permitted. This also means that the FPGA can break a burst transfer into smaller lengths by asserting BTERM. No wait states are generated by the PCI9656 for Space 0 - all wait states are determined by the FPGA.
The Expansion ROM Space is not currently used in the ADM-XRC-II.
The Extra Long Load from Serial EEPROM bit is set to indicate that a long load did occur during the EEPROM read cycle. The length of the EEPROM load is determined by the contents of the EEPROM.

Notes.

1. The bus width of memory space 0 is set to 32 bits by default. As this region is totally under control of the FPGA, it may be changed. It is the responsibility of the FPGA designer to take this into account.
2. The Extra Long Load from Serial EEPROM bit indicates that the extended EEPROM load was performed. This is required to set up Space 1 and some other registers.
3. Expansion ROM Space is not implemented in the ADM-XRC-II and should not be altered.

9.2.4. Direct Master PCI Remap Register

This register is for Local Bus initiated PCI Bus transactions (Direct Master) and is not used in the ADM-XRC-II.

9.2.5. DM Config/IO Register

The DM (Direct Master) Config/IO register is used for controlling configuration cycles on the PCI bus. It is not used in the ADM-XRC-II.

9.2.6. Region 1 Descriptor

The Region 1 Descriptor describes the attributes of Local Bus Space 1. It can be seen that 8 bit local bus width is selected and that ready must be generated by the target space. Burst transfers are not enabled in this space to avoid any side effects of prefetching from control and /or FPGA configuration registers.
Space 1 maps the flash memory, control registers and FPGA SelectMAP port.

Notes.

1. Do not enable burst for this region as it may cause side effects that will stop FPGA loading and readback.
2. Internal wait states should always be 0.
3. Bus width is always 8 bit.

9.2.7. Runtime Registers

The runtime registers group together mailboxes, control and status registers. The only registers applicable to the ADM-XRC-II in this group are the INTCSR register at offset 68h and CNTRL at offset 6Ch.

It should be noted that Mailbox 0 and 1 can be set to initial values using the EEPROM.

9.2.8. Interrupt Control/Status Register

In order to for a PCI host processor to receive interrupts from the many sources in the PCI9656, the appropriate enable bits in the INTCSR must be set.

Notes.

1. Refer to the PLX user manual for the actual register format.
2. Clearing a bit in this register does not remove the interrupting source, it simply masks it.

9.2.9. EEPROM, PCI, User IO

This register is known as CNTRL and reports information about the state of the EEPROM interface, DMA transfer codes and general purpose input and output bits.

Notes.

1. A fault with the EEPROM or if the EEPROM is blank will result in the **Serial EEPROM Present** bit being cleared.
2. This register can be used to write and read the EEPROM for initial programming or to perform changes to the initialisation code.

10. EEPROM Contents

There is a utility in the SDK that can be used to view and change the contents of the EEPROM. As this device contains PLX PCI9656 initialisation data users must be careful about the changes made.

11. FPGA Pin Locations

Refer to the SDK which contains UCF files for various local bus, SRAM and IO configurations.

Revision History

Date	Revision	Nature of Change
July-2001	1.0	Initial draft
Nov-2001	1.1	Updates - I/O modules - Flash Page Info - PLX Configuration register info - SRAM Clocking
Dec-2001	1.2	Updates - XRM IO146 Rev 2.0 added
Feb-2002	1.3	Updates - I/O UCF / FPGA pin cross reference
June-2002	1.4	Updates - Reflects Rev 3 PCB changes for correcting +ve and –ve pin swap on user 140/141 and 123/124
July-2002	1.5	Updates - FPGA Space correction to 4MBytes - Local Bus Speed correction to 66MHz